Litho today, litho tomorrow

Martin van den Brink
President & Chief Technology Officer

31 October 2016
Overview

Industry trends

- Application trends and economics in our ecosystem are driving increasing demand for processing power, high-speed memory, and low-cost storage, fueling the continuation of Moore’s law

Semiconductor impact

- Continuation of Moore’s law will be supported by improving patterning solutions, achieving fast yield ramp-up, to realize attractive economics

Strategic priorities

- As a result, our strategic priorities are: EUV industrialization, DUV competitiveness, leadership in Holistic lithography and EUV extension with High NA

Lithography Roadmap

- We have underpinned our priorities with a detailed product roadmap
The world before 1965 was already on a Moore’s like law … computing speed/€ had been doubling every 2 years for 65 years

Source: Ray Kurzweil
When ASML started Moore’s law was effective for 84 yrs

Calculations per second per $1000

Source: Ray Kurzweil
Today Moore’s law is effective for 116 years
Can exponential curves continue forever?
Moore’s Law is likely not slowing down as long as new idea’s

Source: Ray Kurzweil
Long term multi-decade device roadmap
Substantial performance gain next to the impact of geometric scaling

Every scaling innovation multiplies the value provided by our geometric scaling

Source: John Kelly III, IBM, December 2015
Application trends in our industry drive continued demand for Moore’s Law

### Industry trends towards 2020 and beyond

- **50B connected Internet of Things** devices – needing low-cost devices and generating large data volumes requiring storage and processing
- **89 million connected cars** on the road of which 6 million **self-driving** – generating and processing >1 GB of data per second each
- **250 million personal health** wearables and connected pharmaceuticals for health data collection
- **Explosion of (mostly unstructured) data**, growing to >40 Zetabytes from 5 Zetabytes today

...drive a reinforcing cycle of data creation, transmission, storage and processing...

- **Very high volumes of low-cost semicon devices**
- **Massive computing power and performance memory** in-cloud and in-vehicle
- **Ultrafast & high-band-width network infrastructure**
- **Explosion of high-performance storage capacity**

...driving demand for both low-cost and high performance semiconductor products in both memory and logic

...enabled by the continuation of Moore’s law...

...which underpinned by an ecosystem with combined profits of >290B$
Geometrical scaling critical in support of Moore’s law
now enabled through 4 engines of innovations

Geometric scaling
2D shrink through patterning

Circuit scaling
System-on-chip and advanced packaging

Device scaling
New devices and materials

Architecture scaling
Solution optimization

Source: IMEC, customers
Logic device and shrink roadmap
New devices for 5 nm and beyond are demonstrated to work

<table>
<thead>
<tr>
<th>Year</th>
<th>Logic</th>
<th>Gate length, μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>Planar</td>
<td>32 nm</td>
</tr>
<tr>
<td>2015</td>
<td>FinFET</td>
<td>14 nm</td>
</tr>
<tr>
<td>2020</td>
<td>Horizontal Nanowire</td>
<td>5 nm</td>
</tr>
<tr>
<td>2025</td>
<td>Vertical Nanowire</td>
<td>~2.5 nm</td>
</tr>
<tr>
<td>&gt;2025</td>
<td></td>
<td>~1 nm</td>
</tr>
</tbody>
</table>

Improved performance

Nanowire device structure enables further reduction of gate lengths

Switching threshold, mV/V

- FinFET (width 10nm)
- FinFET (width 5nm) lot 2
- GAA (lot 1, HIGH GP)

Source: IMEC

Scaling of devices is enabled by materials innovation:
- High-K
- III-V

One nanometer transistor, UC Berkeley
Large innovation ongoing in memory, driving continued litho demand

NAND displacing hard disks, 3D NAND displacing 2D NAND, significant integration challenges

Alternative technologies (e.g., CBRAM, PCRAM) likely high litho volume and performance

Source: Western Digital
Solid state replacing high performance disk memory
And new memory technologies to drive the overall performance

Performance metrics:
- Low Latencies
- High IOPS

Source: Will Akin, Micron, Short Course, IEEE IMW may 2016
EUV could simplify customers’ patterning process

Spacer process makes 1D grids with high resolution

Cross section view

- litho
- hard mask

Deposition

- spacer deposition

Etch

- Etch step 1
- Etch step 2

Litho-etch process makes 2D patterns

Top view

- Litho step 1
- Litho step 2

Resolution

Litho critical dimension / $2^n$

Litho critical dimension / $\sqrt{n}$

Final pattern

Top view

Note: process schematics are simplified for presentation purposes

Pitch

Litho critical dimension
Edge placement error & litho critical dimension challenges are main factors for continued shrink.

Edge placement error (EPE) and litho critical dimension (CD) main patterning parameters...

...and shrink requires ever tighter requirements.

- Edge placement error (EPE): combined error of overlay and CD uniformity
- CD uniformity error
- Overlay error

Intended cut

Smaller litho critical dimension needed

Better EPE performance needed (overlay and CD control)
Single Exposure lithography is most attractive optimizing cost, cycle time, yield and edge placement challenges.

<table>
<thead>
<tr>
<th></th>
<th>Cost</th>
<th>Process complexity</th>
<th>EPE complexity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single expose (SE)</td>
<td>✔</td>
<td>✔</td>
<td>-</td>
</tr>
<tr>
<td>Litho etch (LE\textsuperscript{x})</td>
<td>~</td>
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</table>
## Industry Shrink Roadmap & EUV Insertion

<table>
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</thead>
<tbody>
<tr>
<td>Planar Floating Gate NAND</td>
<td>...</td>
<td></td>
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<td></td>
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<td></td>
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<td></td>
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<td></td>
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<tr>
<td>3D NAND</td>
<td>[x24] [x32] [x48] [x64]</td>
<td></td>
<td>&gt;x96</td>
<td>&gt;x128</td>
<td>&gt;x192</td>
<td>&gt;x200</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRAM</td>
<td>[28-30] [20-22] [1X]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PC-RAM, ReRAM, X-point etc.</td>
<td>2X'/x2 1X”/x4 1Y”/x8 1Z”/x8</td>
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<td></td>
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</table>

### EUV Production Insertion Window

<table>
<thead>
<tr>
<th>Node name</th>
<th>Minimum half pitch /x number of layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>3nm</td>
<td></td>
</tr>
<tr>
<td>5nm</td>
<td></td>
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<tr>
<td>7nm</td>
<td></td>
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<tr>
<td>10nm</td>
<td></td>
</tr>
<tr>
<td>14nm</td>
<td></td>
</tr>
</tbody>
</table>

*Source: 1) Customers - public statements, IC Knowledge LLC; 2) ASML extrapolations*
## Strategic priorities to meet customer requirements

Grow our Litho business by delivering superior customer value

<table>
<thead>
<tr>
<th>1</th>
<th>EUV industrialization</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• Deliver high volume manufacturing performance metrics</td>
</tr>
<tr>
<td></td>
<td>• Enhance EUV value for future nodes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2</th>
<th>DUV competitiveness</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• Drive <strong>DUV performance</strong></td>
</tr>
<tr>
<td></td>
<td>– Continue to lead in innovation</td>
</tr>
<tr>
<td></td>
<td>– Drive operational excellence</td>
</tr>
<tr>
<td></td>
<td>– Expand installed base business</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>3</th>
<th>Holistic Litho</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• Build a winning position in <strong>Pattern Fidelity Control</strong> leveraging inspection combined with superior computational Litho</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>4</th>
<th>EUV extension</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• Deliver <strong>High-NA EUV</strong> in time to support customer roadmaps and avoid complex and costly alternatives</td>
</tr>
</tbody>
</table>
EUV key to drive cost effective device shrink roadmaps and simplifying immersion multiple patterning

<table>
<thead>
<tr>
<th>DRAM Active Cut</th>
<th>Node</th>
<th>D20-22</th>
<th>D1X</th>
<th>D1Y</th>
<th>D1Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>ArFi 1.35 NA</td>
<td>SE</td>
<td>LE²</td>
<td>PD+LE²</td>
<td>PQ+LE²</td>
<td></td>
</tr>
<tr>
<td>EUV 0.33 NA</td>
<td></td>
<td></td>
<td></td>
<td>SE</td>
<td>SE</td>
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</tbody>
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<thead>
<tr>
<th>Logic Cuts &amp; Vias</th>
<th>Node</th>
<th>16-14 nm</th>
<th>10 nm</th>
<th>7 nm</th>
<th>5 nm</th>
</tr>
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<tbody>
<tr>
<td>ArFi 1.35 NA</td>
<td>LE²</td>
<td>LE³</td>
<td>LE³⁻⁴</td>
<td>LE⁶⁻⁸</td>
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</tr>
<tr>
<td>EUV 0.33 NA</td>
<td></td>
<td></td>
<td>SE</td>
<td>SE</td>
<td></td>
</tr>
</tbody>
</table>

PoR, Process of Record  
Plan  
Possible but challenging

SE = Single Exposure, LEⁿ = Litho-Etch, n # repeats, PD = Pitch Doubling, PQ = Pitch Quadrupling
EUV industrialization: productivity and consistency

>1500 wafers per day at customer fab, variability needs improvement

System average availability at customer site

3 day average 1,500 wafer per day at customer site

Source: Britt Turkot, Intel, 2016 international symposium on EUV, 24 October 2016, Hiroshima

Source: TSMC, Semicon Taiwan, Sep 2016

- Source: NXE:3350B
- Each bar represents customer wafers exposed on one individual day
We will deliver continued reliability improvement and ramp up our operations to realize EUV in volume manufacturing

### EUV will drive costs and process complexity down for our customers

<table>
<thead>
<tr>
<th>All ArFi</th>
<th>With EUV</th>
</tr>
</thead>
<tbody>
<tr>
<td>2,505</td>
<td>1,743</td>
</tr>
<tr>
<td>34%</td>
<td>50%</td>
</tr>
</tbody>
</table>

Patterning cost per wafer 5nm, €
- Litho CapEx
- Non-litho CapEx
- Opex

-30%

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### … and has made good progress in productivity and reliability

**Productivity**

<table>
<thead>
<tr>
<th>Wafers/day at customer site</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
</tr>
<tr>
<td>&gt;500</td>
</tr>
</tbody>
</table>

**2016 Target:** 1,500

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**Reliability**

<table>
<thead>
<tr>
<th>%, max avg 4 wk availability of installed base</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
</tr>
<tr>
<td>51</td>
</tr>
</tbody>
</table>

**2016 Target:** 80%

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### … triggering increased customer demand

- **“We plan to **extensively use EUV** in 5nm to improve density, simplify process complexity, and reduce cost…Recently EUV development gained quite a good momentum across the industry.”**
  - Mark Liu, co-CEO TSMC, July ‘16

- **“Samsung fully intends to **deploy EUV** for 7nm, triple patterning is not viable …”**
  - “We expect production in 2018”
  - AnandTech & SemiconWest ‘16

- **“Significant strides have been made … taking the technology from a question of **if** to a question of **when. EUV is solidly on a path to HVM insertion** as soon as the technology becomes ready and cost effective”**
  - Intel, SPIE ‘16

Source: ASML, public statements
Drive DUV Competitiveness

DUV competitiveness...

...Our customers
- Enable our customers to execute their roadmaps cost effectively

...Ourselves
- Maintain our market share and margins

DUV Strategic Priorities

<table>
<thead>
<tr>
<th></th>
<th>NXT (Immersion)</th>
<th>XT (Dry)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Leadership</td>
<td>Execute roadmap of next generation products and options aligned with customer priorities</td>
<td></td>
</tr>
<tr>
<td>Operational Excellence</td>
<td>Deliver high quality cost effective solutions</td>
<td></td>
</tr>
</tbody>
</table>
## TWINS CAN Immersion system roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>Products</th>
<th>WpH</th>
<th>Overlay [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>NXT:1950i</td>
<td>190</td>
<td>7</td>
</tr>
<tr>
<td>2011</td>
<td>NXT:1960Bi, NXT:1965Ci</td>
<td>230, 250</td>
<td>6</td>
</tr>
<tr>
<td>2013</td>
<td>NXT:1970Ci</td>
<td>275</td>
<td>4</td>
</tr>
<tr>
<td>2015</td>
<td>NXT:next1, NXT:next2</td>
<td>&gt;285</td>
<td>3, &lt;3, &lt;2</td>
</tr>
</tbody>
</table>

*At customer upgradable products under study*

*Roadmap: October 2016*
Improvements on Next Generation products
Overlay, DUV to EUV matching

- Process robust Alignment improves overlay performance
- Process robust Leveling Improves machine matching
- Wafer Handler Improves overlay performance
- Projection Lens Optimization of lens for improved imaging and overlay
- Improved Grid Setup Improved overlay and machine matching
- Wafer heating control Improved overlay performance
- Wafer table Improved machine matching

Overlay - general
Imaging/Focus
Alignment process robustness improvement
Using multiple wavelengths & polarizations; applicable for DUV and EUV

Using existing sensor at 0° and 90° wafer rotations

Measured Overlay 11.6 nm, 7.5 nm
Measured Overlay 6.7 nm, 6.14 nm

2x process robustness reduction
5x process excursion reduction

Current alignment sensor
+ 2 polarizations and improved algorithms
+ intensity information improved algorithms

Best Color
Color weighting

30 different process stacks and marker combinations in both FEOL and BEOL
Improved focus and leveling process robustness
Through optimized spectrum & angle of incidence; applicable to DUV & EUV
TWINSCAN Dry system roadmap

Continued improvements in productivity and capability of all 4 product lines


- 60nm: XT:400H 365 nm, PEP, XT:400K, PEP, XT:400L, TOP
- 14nm: XT:1000H 248 nm, PEP, TOP
- 10nm: XT:1450H 193 nm, PEP, TOP
- 9nm: XT:1460K, TOP
- 7nm: TOP
- 6nm: TOP, TOP
- 5nm: TOP, PEP

Overlay improvement: PEPE,

Productivity improvement: TOP

Roadmap: October 2016
ASML Holistic Lithography integrates 3 competences
Resulting in 3 customer value propositions

1. Process Window Detection
   - Lithography scanner with advanced control capability
     (imaging, overlay and focus)

2. Metrology
   - Metrology process robust target and recipe creation, ebeam model calibration and computational guided detection.

3. Computational Lithography
   - Other patterning tools

4. Process Window Enhancement
   - Stepper set up and layout optimization for maximum process window

5. Process Window Control
   - Stepper control through on-product overlay, focus and pattern fidelity feedback loops.

6. Other patterning tools
3.2 YieldStar: Unique on product overlay metrology measuring overlay of actual device features, DRAM example

- Negative Overlay
- Zero Overlay
- Positive Overlay

Simulation Result
- Pupil Asymmetry

Simulations show simplified model shows good sensitivity to overlay Translating to ~0.3nm precision

Set/Get Overlay +/- 5.2nm
98% Yieldstar Accuracy (Slope)

Yieldstar ARO SET-GET +/- 5.2nm
Slope = 0.9087
R^2 = 0.9674

CD-SEM

DECAP - SET/GET Result +/- 5.2nm
Slope = 0.7876
R^2 = 0.9487
3.3 Unique Negative Tone resist modelling capability
Modelling accuracy improved 60%

Model error (simulated CD – wafer CD) comparison between empirical NTD model and physical resist shrinkage model.

- **NTD**: the same features are printed in positive resist using light-field masks, with consequently better image contrast; with NTD the exposed resist areas remain intact.
- However, this approach involves additional processing steps (typically coating, baking, etching) and the exposed area is affected in 3 dimensional ways (see open arrows).

- **Physical NTD resist model** accounts for 3 dimensional shrink impacting 2D OPC accuracy.
- **Empirical NTD resist model** does not capture 3 dimensional shrink impact.

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**Customer’s patterns**

**Representative 2D patterns**

**1D patterns**
ASML holistic lithography at 1x nm node: Overlay Control

1. Scanner Control
2. After Litho YieldStar Metrology
3. Computational Lithography

Pre-Holistic Lithography:
- 2xnm node Overlay Requirement
- Other overlay contribution
- Scanner overlay contribution
- Reference: 2xnm node
- 1xnm node scanner improvement only
- Holistic Lithography
- Rework & Yield

Holistic Lithography:
- 1xnm node Overlay Requirement
- Other overlay contribution
- Scanner overlay contribution
- 1xnm node Holistic Lithography
- Rework & Yield

October 31, 2016
ASML holistic lithography future - Pattern fidelity control

- Scanner Control
- Scanner metrology (100% wafers)
- After Litho YieldStar Metrology
- After Litho / Etch E-beam Metrology
- Guide to areas of interest
- Improved models
- Computational Lithography

Guide to areas of interest

October 31, 2016

Public Slide 31

ASML
ASML holistic lithography future: Pattern fidelity control: reducing pattern errors up to ~50% and reduce pattern error by ~50% by control.
EUV with high-NA key to extending device shrink roadmaps and simplifying multiple patterning

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<td>ArFi 1.35 NA</td>
<td>LE²</td>
<td>LE³</td>
<td>LE³-4</td>
<td>LE⁶-8</td>
<td>LE⁸-11</td>
<td></td>
</tr>
<tr>
<td>EUV 0.33 NA</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>EUV &gt;0.5 NA</td>
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SE = Single Exposure, LEⁿ = Litho-Etch, n # repeats, PD = Pitch Doubling, PQ = Pitch Quadrupling

PoR, Process of Record | Plan | Possible but challenging
High NA delivers value to our customers through process simplification, patterning cost and further shrink:

- **High NA simplifies process technology**
  - # of passes, <5 nm node
  - No high NA: 92, With High NA: 62
  - Faster yield-roadmap
  - Faster cycle time
  - Easier node transition

- **... it reduces patterning cost**
  - Patterning cost per layer, EUR
  - 0.33 double patterning
  - 0.55 single exposure
  - 42% cost reduction

- **... and delivers continuation of shrink roadmap**
  - Relative cost per function, %
  - Source: ASML

1 SE = single exposure, LE2 = double patterning;
High-NA optics design concepts available
Larger elements with tighter specifications

Resolution = $k_1 \times \frac{\lambda}{\text{NA}}$

- **Reticle level**
  - NA 0.25
  - NA 0.33
  - NA >0.5

- **Wafer level**
  - NA 0.25
  - NA 0.33
  - NA >0.5

**Design examples**

- Extreme aspheres enabling further improved wavefront / imaging performance
- Tight surface specifications enabling low straylight / high contrast imaging
- Big last mirror driven by High NA
- Obscuration enables higher optics transmission ➔ Potential of up to 2x vs 3300

Anamorphic High NA EUV reduces the angles enabling a solution with 26 mm slit on 6” masks.

Projection with 0.33 NA
Mag X: 4x
Mag Y: 4x

Reticle layout compatible with today 6” mask production

Source: Jan van Schoot, ASML, “EUV roadmap extension by higher Numerical Aperture”, 2016 international symposium on EUV, 24 October 2016, Hiroshima
Anamorphic High NA EUV reduces the angles enabling a solution with 26 mm slit on 6” masks

Reticle layout compatible with today 6” mask production

Projection with >0.5 NA
Mag X: 4x
Mag Y: 4x

Source: Jan van Schoot, ASML, “EUV roadmap extension by higher Numerical Aperture”, 2016 international symposium on EUV, 24 October 2016, Hiroshima
Anamorphic High NA EUV reduces the angles enabling a solution with 26 mm slit on 6” masks

Reticle layout compatible with today 6” mask production

Projection with >0.5 NA
Mag X: 4x
Mag Y: 8x

Source: Jan van Schoot, ASML, “EUV roadmap extension by higher Numerical Aperture”, 2016 international symposium on EUV, 24 October 2016, Hiroshima
Anamorphic optics are used in cinematography

“Don’t change the mask”
High-NA delivers higher throughput

High-NA vs. 0.33NA throughput at given dose

At any power / dose, High NA delivers higher throughput than 0.33NA due to:
- Higher lens transmission
- Improved stage speeds

Source: ASML
## EUV extension roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>Introduction</th>
<th>55 WPH</th>
<th>125 WPH</th>
<th>145 WPH</th>
<th>185 WPH</th>
<th>Overlay [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2013</td>
<td>NXE:3300B</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>2015</td>
<td>NXE:3350B</td>
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<td>3.5</td>
</tr>
<tr>
<td>2017</td>
<td>NXE:3400B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3</td>
</tr>
</tbody>
</table>

At customer upgradable

New platform

products under study

**Roadmap: October 2016**
The future

• **Moore’s law to continue for the foreseeable future**, driven by connecting everything around us, generating massive data and enabled by geometrical device, architectural and circuit scaling. Logic device innovation and memory/computer architecture innovations in support of this.

• **EUV industrialization** enabled by identified insertion opportunity at multiple customers and execution to roadmaps progressing to plan, improvements still needed for consistency.

• **DUV competitiveness** to support continued demand given its cost advantage over EUV for less critical layers and some double patterning. Improvements in CD and overlay continued to be required for future nodes.

• **Holistic Lithography** is being extended with pattern fidelity control. Metrology extensions needed for on product robust process, after etch targets and resolution enhancements through computational enhanced e-beam capability. Increased scanner control capability to enable ultimate on product process control.

• **EUV extension** with high NA enable cost-effective shrink to continue into the next decade
Forward looking statements

This document contains statements relating to certain projections and business trends that are forward-looking, including statements with respect to our outlook, including expected customer demand in specified market segments (and underlying assumptions) including memory, logic and foundry, expected sales levels, trends, including trends towards 2020 and beyond and expected industry growth, and outlook, systems backlog, expected or indicative market opportunity, financial results and targets, including, for ASML and ASML and HMI combined, expected sales, other income, gross margin, R&D and SG&A expenses, capital expenditures, cash conversion cycle, EPS and effective annualized tax rate, annual revenue opportunity and EPS potential by end of decade and growth opportunity beyond 2020 for ASML and ASML and HMI combined, cost per function reduction and ASML system ASP, goals relating to gross cash balance and ASML’s capital structure, customer, partner and industry roadmaps, productivity of our tools and systems performance, including EUV system performance (such as endurance tests), expected industry trends and expected trends in the business environment, the addition of value through delivery of lithography products and the achievement of cost-effective shrink, expected continued lithography demand and increasing lithography spend, the main drivers of lithography systems, lithography intensity for all market segments, customer execution of shrink roadmaps, future memory application distribution, expected addressable markets, including the market for lithography systems and service and options, expected manufacturing and process R&D, statements with respect to growing end markets that require fab capacity driving demand for ASML’s tools, statements with respect to the acquisition of HMI by ASML, including market opportunity, the expected timing of completion of the HMI acquisition and delisting of HMI, the expected benefits of the acquisition of HMI by ASML, including expected continuation of year on year growth, the provision of e-beam metrology capability and its effect on holistic lithography solutions, including the introduction of a new class of pattern fidelity control and the improvement of customers’ control strategy, statements with respect to EUV, including targets, such as availability, productivity, facilities and shipments, including the number of EUV systems expected to be shipped and timing of shipments, and roadmaps, shrink being key driver to industry growth, expected industry adoption of EUV and statements with respect to plans of customers to insert EUV into production and timing, the benefits of EUV, including expected cost reduction and cost-effective shrink, the expected continuation of Moore's law, without slowing down, and that EUV will continue to enable Moore’s law and drive long term value, goals for holistic lithography, including pattern fidelity control, expectations relating to double patterning, immersion and dry systems, intention to return excess cash to shareholders, statements about our proposed dividend, dividend policy and intention to repurchase shares and statements with respect to the current share repurchase plan. You can generally identify these statements by the use of words like “may”, “will”, “could”, “should”, “project”, “believe”, “anticipate”, “expect”, “plan”, “estimate”, “forecast”, “potential”, “intend”, “continue” and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them.

Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors (the principal product of our customer base), the impact of general economic conditions on consumer confidence and demand for our customers’ products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of new products including EUV, the number and timing of EUV systems expected to be shipped and recognized in revenue, delays in EUV systems production and development, our ability to enforce patents and protect intellectual property rights, the risk of intellectual property litigation, availability of raw materials and critical manufacturing equipment, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases and timing of resumption of the share repurchase plan, and other risks indicated in the risk factors included in ASML’s Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.