Many ways to shrink: The right moves to 10 nanometer and beyond

Martin van den Brink
President & Chief Technology Officer

24 November 2014
Content

• **Industry Challenges**
  - The desire to shrink
  - The device challenges
  - The scaling challenges

• **ASML Solutions**
  - Our holistic approach to extend immersion
  - The process simplification by using EUV
Moore’s Law: the rice-and-chessboard challenge
The benefits of shrink are irresistible
Driving the semiconductor industry: Moore’s Law; “…home computers…and personal portable communication…”

Gordon Moore’s prediction, 1965

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Reality, ~ 50 years later, 2014

Some question if Moore’s Law can continue

End of Moore’s Law: It’s not just about physics

A DARPA director argues that the end of the Moore’s Law – which why you don’t have a tablet in your hand – could come about because of unbreakable economic challenges.

Intel: The End Of Moore's Law

OK, OK, so we are not yet at the end of Moore’s Law and from here. Moore’s Law comes to us from Gordon Moore, the founder of Integrated Semiconductor (ICS) and later, Intel Corporation. Moore wrote a paper in 1965 describing his transistors on a given cost integrated circuit invention of the integrated circuit, and his idea was to double, at the same cost, the size of a transistor. The same detail that哪 discussions of Moore’s Law is that the next generation of transistors will not be cheaper. So the size of a transistor has to keep getting more expensive.

Cost per Million Gates (b)

<table>
<thead>
<tr>
<th>Technology</th>
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Mobile applications continue to be on an yearly cadence device and litho innovations driving area, power and performance.

Source: Esin Terzioglu, Qualcomm, EUV symposium, Oct 2014
Mobile chips integrating functionality faster than shrink
Apple: first high volume 20nm process in the iPhone 6(+)

Apple A4
1-Core and 1-GPU
53 mm² – 45 nm

Apple A5
2-Core and 2-GPU
needed for iPad Display
122 mm² – 45 nm

Apple A5X – iPad 3
2-Core and 4-GPU
needed for Retina Display
169 mm² – 45 nm

Apple A5S – AppleTV, iPad2, iPad Mini, iPod Touch
70 mm² – 32 nm

Apple A5S – AppleTV, iPad2, iPad Mini, iPod Touch
70 mm² – 32 nm

Apple A6
New Dual Core and 3-GPU
needed for Retina Display
97 mm² – 32 nm

Apple A7 - iPhone 5S & iPad Air
Two 64bit cores
1 Billion transistors
102 mm² – 28 nm Apple

Apple A8 iPhone 6/6+
2-core 64bit & 4-GPU’s
90 mm² – 20 nm

Apple A6X
New Dual Core and 4-GPU
needed for Retina Display iPad 4
123 mm² – 32 nm

Apple A9X
New Dual Core and 4-GPU
needed for Retina Display iPad 4
123 mm² – 32 nm

Apple A8X
New Dual Core and 4-GPU
needed for Retina Display iPad 4
123 mm² – 32 nm

Apple A9
Two 64bit cores
2 Billion transistors
90 mm² – 32 nm

Apple A10
Two 64bit cores
3 Billion transistors
68 mm² – 20 nm Apple

Source: Apple
And area and cost per function reduction accelerates

And is a competitive item between chip makers.

Source: ¹Bill Holt, Intel investor conference, Nov 2013
²Mark Liu, TSMC analyst call, Jan 2014
The challenge of Moore’s law chessboard in numbers

What about our customers challenges?

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<td>9.22E+18</td>
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</table>
Shrink scenarios for logic devices

Bulk CMOS at 100 nm gate length: open

Bulk CMOS at 100 nm gate length: closed

N20

N20 / N14

N10

N20 / N7

N7 / N5

N5 / N3.5

Bulk CMOS: Complementary Metal Oxide Semiconductor

SOI: Partially depleted Silicon on insulator

SOI: Fully depleted Silicon on insulator

Bulk FinFet: fin field effect transistor

SOI FinFet: silicon on insulator fin field effect transistor, III-V

Gate-all-around transistor
Shrink scenarios for logic devices

Bulk CMOS 20 nm: open
Bulk CMOS 20 nm: closed

N 20
N 20 / N 14
N 10
N 20 / N 7
N 7 / N 5
N 5 / N 3.5

Bulk CMOS: Complementary Metal Oxide Semiconductor
SOI: Partially depleted Silicon on insulator
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Bulk FinFet: fin field effect transistor
SOI FinFet: silicon on insulator fin field effect transistor, III-V
Gate-all-around transistor
Shrink scenarios for logic devices

Solution 1:

- **Silicon on insulator (SOI):**
  - Partially depleted Silicon on insulator
  - Fully depleted Silicon on insulator

- **Bulk CMOS:** Complementary Metal Oxide Semiconductor
- **SOI FinFET:** silicon on insulator fin field effect transistor, III-V
- **Bulk FinFET:** fin field effect transistor
- **Gate-all-around transistor**

**Specifications:**
- N 20
- N 20 / N 14
- N 10
- N 20 / N 7
- N 7 / N 5
- N 5 / N 3.5
Shrink scenarios for logic devices

Solution 2:

- **Bulk FinFet**
  - **SOURCE**
  - **GATE**
  - **DRAIN**

**Bulk CMOS:** Complementary Metal Oxide Semiconductor

- **N 20**
- **N 20 / N 14**
- **N10**
- **N 20 / N 7**
- **N 7 / N 5**
- **N 5 / N 3.5**

**SOI:**
- **Partially depleted Silicon on insulator**
- **Fully depleted Silicon on insulator**

**SOI FinFet:**
- silicon on insulator fin field effect transistor
- silicon on insulator fin field effect transistor, III-V

**Gate-all-around transistor**
Shrink scenarios for logic devices

Gate all around: Open

Gate all around: Closed

**Bulk CMOS:** Complementary Metal Oxide Semiconductor

**SOI:** Partially depleted Silicon on insulator

**SOI:** Fully depleted Silicon on insulator

**Bulk FinFet:** fin field effect transistor

**SOI FinFet:** silicon on insulator fin field effect transistor, III-V

Gate-all-around transistor
No end in sight for logic scaling

N 20
Bulk CMOS: Complementary Metal Oxide Semiconductor

N 20 / N 14
SOI: Partially depleted Silicon on insulator

N 10
SOI: Fully depleted Silicon on insulator

N 20 / N 7
Bulk FinFet: fin field effect transistor

N 7 / N 5
SOI FinFet: silicon on insulator fin field effect transistor, III-V

N 5 / N 3.5
Gate-all-around transistor
Significant architectural innovations ahead for Memory

Source: Meng-Fan Chang, NTU Taiwan, Resistive memory workshop, Stanford, Oct 2014
2D NAND vs 3D V-NAND Challenges

2D Cell to cell interference

- Over 30nm
- D/R Over 30nm
- Over 30nm

3D Aspect ratio

- Over 30nm

Source: Jung, Samsung, Flash Memory Summit, Santa Clara, Aug 2013
NAND memory continuing on multiple fronts
2D extensions, 3D introduction and ReRam coming

Source: Siva Sivaram, Sandisk investor day presentation, May 2014.
NAND memory continuing on multiple fronts
2D extensions, 3D introduction and ReRam coming

Source: Siva Sivaram, Sandisk investor day presentation, May 2014.
NAND memory continuing on multiple fronts
2D extensions, 3D introduction and ReR Ram coming

Source: Siva Sivaram, Sandisk investor day, May 2014
Scott DeBoer, Micron investor day, Aug 2014
Critical requirements for scaling 3D memory devices
Etch aspect ratio vs litho scaling cost challenge

**Vertical NAND**
- Gates around conductive vertical channel
- Lithography light, critical overlay to top layer
- Deposition and deep etch intensive, horizontal density limited due to etch aspect ratio. Key: deep contact etch
- Large gate size

**Cross bar ReRAM**
- Perpendicular gate and channel architecture with horizontal conduction
- Lithography intensive (< 15nm, EUV)
- Deposition and litho etch per layer similar to 2D, density determined by litho
- Scalable gate possible
New memory competes with DRAM and NAND extensions and its likely delayed transition determined by cost scaling.

Source: S.W. Park, Hynix, ITPC Hawaii, Nov 2014
Sub-resolution imaging requires multiple litho steps

<table>
<thead>
<tr>
<th>2D Multi Patterning or EUV single expose</th>
<th>1D Self Aligned Multiple Patterning (SAMP)</th>
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</thead>
<tbody>
<tr>
<td>LELE (or EUV SE)</td>
<td>SADP (D=Double)</td>
</tr>
<tr>
<td>LELELE (or EUV SE)</td>
<td>SAQP (Q=Quadruple)</td>
</tr>
<tr>
<td>LE #1</td>
<td>Mandrel</td>
</tr>
<tr>
<td>LE #2</td>
<td>Spacer</td>
</tr>
<tr>
<td>LE #3</td>
<td>Spacer cut</td>
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<tr>
<td></td>
<td>Patterning cut(s)</td>
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<tr>
<td></td>
<td></td>
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<tr>
<td>Process Flow</td>
<td></td>
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<tr>
<td>LE #1</td>
<td>Mandrel</td>
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<tr>
<td>LE #2</td>
<td>Spacer #1</td>
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<tr>
<td>LE #3</td>
<td>Spacer #2</td>
</tr>
<tr>
<td></td>
<td>Patterning cut(s)</td>
</tr>
</tbody>
</table>

- Suitable for 1D or 2D patterning
- Overlay control of each layer is a key
- Suitable for 1D layout (better CD, LWR control)
- May need multiple cut patterns
10nm logic design can be done in 1D
..but at the penalty of 15% larger die at comparable design rules

2D
Die size: 100%

1D
Die size: 115%
EUV: reduced complexity & design rule simplification
Allowing 2D structures and potentially better yield

Able to employ jogs
Reduced # vias (better yield)
Less min. length (area) wires
Able to connect to neighbor wire

Better freedom for redundant via insertion

Reduced MOL complexity by 2D M1

Source: Esin Terzioglu, Qualcomm, EUV symposium, Oct 2014
10nm patterning choices & cost estimates
EUV lowest cost and complexity for 2D structures

**EUV**
- 2D structure
- Single layer solution
- Cost for 1 layer 100%
  - Good pattern fidelity
  - Re-use existing designs

**ArFi LE^4**
- 2D structure
- Single layer solution
- Cost for 1 layer ~ 170%
  - Insufficient pattern fidelity
  - **NO SOLUTION**

**ArFi – 1D only**
- 6-8 exposures in 3 layers
  - (use separate layers for horizontal and vertical connections)
- Cost for 2-3 layers > 250%
  - 1-2 extra layers needed
  - New integration scheme
  - Significant cost increase
Continued significant cost reduction viewed as possible but significant innovation is needed.

Relative Cost Per Gate at Maturity

Technology Node (nm) 65 45 28 20/14 10 7

- "traditional path"
  - Primary culprit: litho cost
  - New Materials Opportunities
  - Multi-pattern cost down
  - EUV lithography
  - Design/tech co-optimization
  - ....

Source: Esin Terzioglu, Qualcomm, EUV symposium, Oct 2014
EUV supports “free functionality” for the 7nm node

Doubling functionality (2x # gates) node-to-node

“Relative Cost”

N10  N7-193i  N7-EUV LS

Source: Esin Terzioglu, Qualcomm, EUV symposium, Oct 2014
# Industry production roadmap summary

<table>
<thead>
<tr>
<th>Year</th>
<th>NAND / Non Volatile Equivalent Node (Feq) Node = (WL + BL) / 2</th>
<th>DRAM / Volatile Memory Equivalent Node (Feq) HP≥ 79% of Feq</th>
<th>LOGIC Node / Metal-HP [nm]</th>
<th>MPU Node / Metal-HP [nm]</th>
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<tbody>
<tr>
<td>2009</td>
<td>35</td>
<td>52</td>
<td>40 / 70</td>
<td>32 / 60 (planar)</td>
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<td>2010</td>
<td>28</td>
<td>48</td>
<td>32 / 50</td>
<td>22 / 40 (finFET)</td>
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<td>2011</td>
<td>22</td>
<td>38</td>
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<td>2012</td>
<td>19 x 22</td>
<td>33</td>
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<tr>
<td>2013</td>
<td>19</td>
<td>28 (6F²)</td>
<td>20 / 32 (planar)</td>
<td>14 / 30 (finFET)</td>
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<td>2014</td>
<td>16 5x 3D²⁴lyrs</td>
<td>25 (6F²)</td>
<td>14~16 / 32 (finFET)</td>
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<td>2015</td>
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<td>22 (6F²)</td>
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<td>10 / 19 (finFET)</td>
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<td>2016</td>
<td>13 5x 3D⁴⁸lyrs</td>
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<td>7 / 12 (finFET)</td>
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<td>2017</td>
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<td>7 / 16 (finFET)</td>
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<td>2018</td>
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<td>19 MRAM</td>
<td>5 / 11 (finFET)</td>
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<td>2019</td>
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<td>16 STT-MRAM</td>
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<td>2020</td>
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<td>2021</td>
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<td>14 STT-MRAM</td>
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<td>2022</td>
<td>10 ReRAM⁸lyrs</td>
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Note: Node represents start volume (>10% unit share) of the typical customer roadmap

* Q1-2014 customer roadmaps

- **Single expose Pattern split / Cut mask**
- **Double patterning - SPT**
- **Double patterning - LxLE**
- **EUV**
Industry production roadmap summary

<table>
<thead>
<tr>
<th>Date</th>
<th>NAND / Non Volatile Equivalent Node (Feq)</th>
<th>DRAM / Volatile Memory Equivalent Node (Feq)</th>
<th>LOGIC Node / Metal-HP [nm]</th>
<th>MPU Node / Metal-HP [nm]</th>
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- Estimated NAND EUV insertion
- Estimated DRAM EUV insertion
- Estimated Logic EUV insertion
- Estimated MPU EUV insertion

*Q1-2014 customer roadmaps

Note: Node represents start volume (>10% unit share) of the typical customer roadmap

Single expose Pattern split / Cut mask

Double patterning - SPT

Double patterning - LxLE

EUV
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<td>1.07E+09</td>
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</table>

Our customers moved to the second half of the board. During the past 66 years, 1.4 shrink/year, with more moves to come!

Jack Kilby’s first 1 transistor oscillator IC, 1958

- High-end MPU: 5 billion transistors
- 6 Gb DRAM: 6 billion transistors
- High-end GPU: 7 billion transistors
- High-end FPGA: 20 billion transistors

128 Gb SLC NAND: 137 billion transistors

November 2014 Public Slide 33
Customer roadmap summary

• Significant innovation ahead in logic including scaling enabling the continuation of cost reduction for the next 10 years
• Logics environment very competitive relative to manufacturing cost dominated by shrink capability
• Memory roadmap to be diversified through the offering on multiple hardware innovations connected through software
• Continued shrink planned for the next 10 years to drive memory cost delivering power and speed performance in the memory architecture
• EUV to bring process simplicity allowing 2D layout enabling more effective shrink
Content

- Industry Challenges
  - The desire to shrink
  - The device challenges
  - The scaling challenges

- ASML Solutions
  - Our holistic approach to extend immersion
  - The process simplification by using EUV
Multi-patterning complexity explodes using immersion

<table>
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<th>Node</th>
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<td>23</td>
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<tr>
<td># OVL metrology</td>
<td>7</td>
<td>9-11</td>
<td>36-40</td>
<td>59-65</td>
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</tbody>
</table>
Our Challenge: keep scaling affordable

- Scaling needs to create **lower cost and improved performance**

- Affordable scaling in lithography can be achieved:
  - **Holistic Lithography** with both EUV and Immersion to drive on product requirements
  - **Immersion**: drive **productivity and yield (overlay and focus control)** with multiple patterning using advanced litho equipment
  - **EUV**: drive **productivity** and improve **operational cost**
ASML holistic lithography roadmap
Linking the scanner to YieldStar metrology and Tachyon design context

1. Advanced lithography capability (Imaging, overlay and focus)
   - Stepper control through on-product overlay, focus and CD feedback loops window
   - Design context used to identify hotspot and correct them

2. Metrology and control SW

3. BRION Computational lithography

4. Process window enlargement
   - Stepper set up and layout optimization for maximum process window

5. Process window control

6. Process window detection

Product reticles

Product wafers

ASEL November 2014
Public
Slide 38
1) TWINSCAN immersion product roadmap
Enabling extension of customer roadmaps and control capital efficiency

<table>
<thead>
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<th>Application Node</th>
<th>Logic</th>
<th>DRAM</th>
<th>190 WpH</th>
<th>230 WpH</th>
<th>250 WpH</th>
<th>&gt;275 WpH</th>
<th>On product overlay</th>
<th>1st Shipment</th>
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<tbody>
<tr>
<td>Logic</td>
<td>28</td>
<td>2H</td>
<td>NXT:1950i</td>
<td></td>
<td></td>
<td></td>
<td>7 nm</td>
<td>2009</td>
</tr>
<tr>
<td>Logic</td>
<td>2M</td>
<td>2L</td>
<td></td>
<td>NXT:1960Bi</td>
<td></td>
<td></td>
<td>6.5 nm</td>
<td>2011</td>
</tr>
<tr>
<td>Logic</td>
<td>20/16/14</td>
<td>2L</td>
<td>SNEP 1</td>
<td>NXT:1965Ci</td>
<td>NXT:1970Ci</td>
<td>PEP 275</td>
<td>6.5 nm</td>
<td>2013</td>
</tr>
<tr>
<td>Logic</td>
<td>10</td>
<td>1H</td>
<td>SNEP 1</td>
<td>PEP 275</td>
<td></td>
<td></td>
<td>&lt;5 nm</td>
<td>2013</td>
</tr>
<tr>
<td>Logic</td>
<td>7</td>
<td>1M</td>
<td>SNEP 2</td>
<td>NXT:1980Di</td>
<td></td>
<td></td>
<td>&lt;3.5 nm</td>
<td>2015</td>
</tr>
<tr>
<td>Logic</td>
<td></td>
<td></td>
<td>SNEP: System Node Extension Package</td>
<td></td>
<td></td>
<td></td>
<td>2.5 nm</td>
<td>2017</td>
</tr>
<tr>
<td>Logic</td>
<td></td>
<td></td>
<td>PEP: Productivity Enhancement Package</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Public Slide 39
November 2014
2) YieldStar 250D; latest ASML metrology system
Providing Overlay, Focus and CD feedback for scanner control

Illumination
• Laser Pumped Plasma Source
• Narrow and wideband filters
• Wavelength extension to 765nm

Sensor:
• Optics to support wavelengths up to 780nm
• Faster cameras with higher detection efficiency
3) Negative tone develop model validation
10nm node metal layer wafer results (triple patterning, LELELE)

Model calibration RMS: 2nm (1D & 2D), Wafer DOF: 80nm, Across wafer CDU: 1.1nm

Source: Imec
4) Source-mask optimization of flexible illumination improves triple patterning process window >23%

- 10nm node metal1: 48nm min. pitch, 3 splits, NTD and M3D models used
- One common source optimized for best imaging of all 3 splits (LELELE)

Source: Imec
5) 20% improvement in On Product Overlay (per lot) looking at the biggest excursions using integrated metrology

Max Overlay per Lot _X [nm]

<table>
<thead>
<tr>
<th>Standalone metrology Lots</th>
<th>Integrated metrology (IM) Lots</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 scanners, 3 YieldStar S200</td>
<td>5 Litho-clusters with YieldStar T200</td>
</tr>
</tbody>
</table>

20% improvement with IM

Lots run on YieldStar (S on left, T on right, same sampling, same timeframe)

One month production data 2x node BEOL layer

Each data point is one Lot
6) Computational lithography now enters the fab provide metrology context reducing target and recipe design qualification

Overlay simulated and measured on customer product wafers of various markers and recipe combinations

- Physical overlay (measured) vs. Overlay accuracy KPI (simulated)
- Physical overlay (measured) vs. TMU

Physical overlay measurement (SEM)

Overlay accuracy KPI Simulated

Overlay (Accuracy) KPI: \[ \frac{\partial \text{OVL}}{\partial \text{Asym}_i} \]

\[ \text{Asym}_i = \{\Delta \text{SWA}, \text{Floor tilt}, \ldots\} \]

MIN Marker, recipe

Overlay KPI (marker, recipe)
ASML enabled 18 moves on the chessboard in 30 years

1973: 1:1 Scanners,
3 um, 75 mm Wafers, 40 Wafers/hr, 5.4 Mpixel/s

1984: G/H line
1,2 um, 100 mm Wafers, 40 W/hr, 61 Mpixel/s

2014: 193 nm Immersion
19 nm, 300 mm Wafers, 250 W/hr, 14 Tpixel/s

Contact printing
1:1 scanners
DUV step scan or expose and repeat

1958
1973
1984 ASML
2014
Multi-patterning could explode, but EUV will simplify through less patterning and metrology steps.

<table>
<thead>
<tr>
<th>Node</th>
<th>28nm</th>
<th>20nm</th>
<th>10nm</th>
<th>7nm all immersion</th>
<th>7nm all EUV</th>
</tr>
</thead>
<tbody>
<tr>
<td># of lithography steps</td>
<td>6</td>
<td>8</td>
<td>23</td>
<td>34</td>
<td>9</td>
</tr>
<tr>
<td># OVL metrology</td>
<td>7</td>
<td>9-11</td>
<td>36-40</td>
<td>59-65</td>
<td>12</td>
</tr>
</tbody>
</table>
NXE:3300B litho performance proven
Good imaging, overlay and full field pellicles

NXE:3300B, 10 nm logic metal 1 layer example, 45 nm minimum pitch, 1.6 nm RMS

Focus

-60nm

0nm

60nm

Source: ST, 2014

Full size pSi pellicle realized, 103x122 mm, 85% (single pass) transmission mounting an evaluation in progress

EUV to Immersion overlay

Matched Machine Overlay [nm]

Overlay X  Overlay Y

0  0.5  1  1.5  2  2.5  3  3.5  4  4.5  5

1  2  3  4

November 2014

Public Slide 47
NXE:33x0B demonstrated power supports >1000 wpd
Up to 7 systems operational at >40W; 100W source operation demonstrated

- Expose speed
- Expose speed 3350B (calc.)
- Projected WPD

- NXE:33100 Proto
  - Demonstrated WPD at multiple customer sites (@customer conditions)
  - Lot overhead improvements

- NXE:33300B

- NXE:3350B
  - Equivalent Productivity @ 15 ml/cm², 50% efficiency [w/day]

- Dose-to-expose is 2.5x dose-to-clear
- Productivity: field size 26x33 mm², 96 fields/wafer, 50% efficiency
- NXE:3350B data calculated using measured transmission of last system
Multi-patterning planned with EUV on future nodes but…
>0.5 high-NA will simplify and extend roadmap again

<table>
<thead>
<tr>
<th>Node</th>
<th>7nm - EUV</th>
<th>5nm - EUV</th>
<th>3nm - EUV</th>
<th>5nm - high NA EUV</th>
<th>3nm - high NA EUV</th>
</tr>
</thead>
<tbody>
<tr>
<td># of lithography steps</td>
<td>9</td>
<td>12</td>
<td>19</td>
<td>9</td>
<td>12</td>
</tr>
<tr>
<td># OVL metrology</td>
<td>12</td>
<td>18-22</td>
<td>29-36</td>
<td>12</td>
<td>18-22</td>
</tr>
</tbody>
</table>
We are preparing to make another 6 moves in 10 years.
Our next move: 13nm EUV lithography

### 1958
- Jack Kilby's oscillator contains ~50 pixels to be exposed through contact printing in 1 sec.

### 1973
- 1:1 scanners

### 1984
- DUV step scan or expose and repeat

### 2019-2024: 13nm EUV
- 3 nm, 300 mm Wafers, 200 W/hr, 0.45 Ppixel/s

<table>
<thead>
<tr>
<th>Year</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
<th>32</th>
<th>64</th>
<th>128</th>
</tr>
</thead>
<tbody>
<tr>
<td>1958</td>
<td>256</td>
<td>512</td>
<td>1024</td>
<td>2048</td>
<td>4096</td>
<td>8192</td>
<td>16384</td>
<td>32768</td>
</tr>
<tr>
<td>1973</td>
<td>65536</td>
<td>131072</td>
<td>262144</td>
<td>524288</td>
<td>1048576</td>
<td>2097152</td>
<td>4194304</td>
<td>8388608</td>
</tr>
<tr>
<td>1984</td>
<td>1638216</td>
<td>3355443</td>
<td>6710886</td>
<td>13421772</td>
<td>26843544</td>
<td>53687088</td>
<td>107374176</td>
<td>214748368</td>
</tr>
<tr>
<td>2014</td>
<td>4.29E+09</td>
<td>8.59E+09</td>
<td>1.72E+10</td>
<td>3.44E+10</td>
<td>6.87E+10</td>
<td>1.37E+11</td>
<td>2.74E+11</td>
<td>5.5E+11</td>
</tr>
<tr>
<td>2019</td>
<td>1.1E+12</td>
<td>2.2E+12</td>
<td>4.4E+12</td>
<td>8.7E+12</td>
<td>1.76E+13</td>
<td>3.52E+13</td>
<td>7.05E+13</td>
<td>1.41E+14</td>
</tr>
<tr>
<td>2024</td>
<td>2.81E+16</td>
<td>1.13E+17</td>
<td>2.25E+17</td>
<td>4.5E+17</td>
<td>9.01E+17</td>
<td>1.8E+18</td>
<td>3.6E+18</td>
<td>7.21E+18</td>
</tr>
</tbody>
</table>

Contact printing

EUV
Summary

- Node progression enabled by immersion multi pass patterning and extended litho metrology and computational litho to control complexity
- To address highly complex multi-patterning schemes, EUV insertion is likely at the 10nm logic and 7nm MPU node with full production one node later
- ASML has demonstrated consistent EUV source progress. Today performance approaching 100W exposure power. System uptime remains a key challenge
- EUV infrastructure supportive for above transition scenarios
- Lithography roadmap defined down to the 3nm node
Had the King’s name been Moore….

He would have worked to find ways to scale down his grains, keep their nutritional value and double the amount with every move. He could have fed the world, instead of having lost a Kingdom.