Next Generation Lithography
The road to cost-effective shrink

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Agenda

- Shrink roadmap
- Progress in immersion lithography
- A holistic approach to extend immersion lithography
- EUV the next production worthy shrink technology
- Economics of advanced lithography
Shrink will continue
(based on the average of multiple customers’ input)

*Process development 1.5 ~ 2 years in advance (updated 12/07)
## Most likely litho roadmap

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<th>100</th>
<th>65</th>
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<td>0.53</td>
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[Green] most likely
[Orange] opportunity
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Immersion 1.35 NA scalable to 38 nm

- NA = 1.35
- Dipole-X-35 $\sigma = 0.82/0.97$
- Y Polarization
- 6% Att PSM mask

SGL WL1 ...32 parallel word lines
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  - Double patterning
    - Optimize performance using computational lithography
    - Reduce variability using intra-field litho correction
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Options to print below immersion single exposure limit

- **Spacer DPT | SPCR 32nm**
- **Litho DPT - LELE | LDPT 32nm**
- **Litho DPT - LFLE | LDPF 32nm**
- **Double exposure | DE 38 nm**
- **Single exposure | SE 45nm**

- **K1 > 0.25**
  - *Wafer does not leave the exposure system between the two exposures*

- **K1 < 0.25**
  - *Wafer leaves litho cell for etch between the exposures*

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**Cost, complexity and cycle time**

*Wafer does not leave the exposure system between the two exposures*

*Wafer preferably does not leave the litho cell between the exposures*

*Wafer leaves litho cell for etch between the exposures*

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*Wafer does not leave the exposure system between the two exposures*

*Wafer preferably does not leave the litho cell between the exposures*

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Options to print below immersion single exposure limit:

- **SiON /HM Etch**
- **Clean**
- **Strip**
- **Film Etch**
- **Metrology**
- **Develop**
- **Expose**
- **Top coat**
- **Resist**
- **BARC**
- **SiON / SiC**
- **Hard Mask**
- **Device film**
- **Si**

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*Wafer does not leave the exposure system between the two exposures*

*Wafer preferably does not leave the litho cell between the exposures*

*Wafer leaves the litho cell for etch between the exposures*
Single exposure (like EUV): lowest process complexity and most relaxed litho requirements, suitable for 1D and 2D scaling, logic and all memory

Real CD is smaller than target CD. Error caused by litho step

CD error during litho process steps will result in smaller lines

Extra CD errors are created during etch step combined with litho CD error to a final CD error

CD determined by 2 error components litho and etch:

$\Delta C D_{litho} < 7\%$ of CD

Overlay $< 20\%$ of CD
Litho double patterning: Litho-Freeze-Litho-Etch

Litho quality yet below required 32 nm performance but lowest cost opportunity: wafer will not leave the litho cell between the 2 exposures

**Litho 1**
Standard resist

“Freezing” process first developed image:
1) Coat first developed (shown)
2) Thermal treatment
3) Pos/Neg resist
4) Other post development treatment

**Litho 2**
Coat, expose, develop 2\textsuperscript{nd} pattern

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Data generated in collaboration with IMEC
Litho double patterning: Litho-Etch-Litho-Etch

Suitable for 1D and 2D scaling, logic and all memory

1st Photo CD errors during litho will result in smaller/larger lines

1st Etch+CD trim
Extra CD errors could take place

2nd Photo
Overlay error translates into CD error between lines

2nd etch+CD trim
2nd pattern with CD errors from 2nd etch/trim and overlay

Real CD litho is smaller than target CD litho. Error caused by litho

Target CD litho

32 nm lines/96 nm spaces

32 nm lines/32 nm spaces

CD determined by 8 error components; 2 x litho, 2 x etch and overlay:

\[ \Delta CD_{\text{litho}} < 3.5\% \text{ of CD} \]

\[ \text{Overlay} < 7\% \text{ of CD} \]

Final CD < 10% CD
Spacer double patterning litho requirements
1D scaling only, suitable for Flash

Real CD is smaller than target CD. Error caused by litho and etch trim patterning steps

Sacrificial line patterning:
A CD error during litho and etch process steps will result in smaller lines

Line CD error propagates during spacer uniform deposition and etched back

Initial CD error becomes a pitch variation on the final pattern

CD determined by 11 error components; litho, etch, spacer deposition, trim and final etch:
ΔCDlitho < 3 % of CD
Overlay < 20% of CD

Target CD litho

Final CD < 10%CD

Data generated in collaboration with IMEC
Negative spacer flow for NAND periphery

A design → B Pattern split → C 1st litho/etch → D 1st spacer deposition → E 2nd film dep → F 2nd litho/Trim → G After etch

This is the overlap of the trim mask and layout in E

Based on Soo-Han Choi et al. | SPIE Ref. 5377-63
"Simulation-based critical area extraction and litho-friendly layout design for low k₁ lithography"
Double patterning requires better and more lithography

<table>
<thead>
<tr>
<th>Litho exposure equipment parameter as percentage of CD</th>
<th>Single exposure</th>
<th>Litho double patterning</th>
<th>Spacer double patterning</th>
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<tr>
<td>ΔCD</td>
<td>7%</td>
<td>3.5%</td>
<td>3%</td>
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<tr>
<td>Overlay (depending on DFM)</td>
<td>20%</td>
<td>7%</td>
<td>7-20%*</td>
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<tr>
<td># mask steps</td>
<td>1</td>
<td>2</td>
<td>2-3</td>
</tr>
<tr>
<td># process steps relative to single exposure</td>
<td>1</td>
<td>2</td>
<td>3-4</td>
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<tr>
<td>Application</td>
<td>2D, all</td>
<td>2D, all</td>
<td>1D, mainly memory</td>
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</tbody>
</table>

* Depending on the amount of “Design For Manufacturing” effort
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Low $k_1$: High design to wafer integration

Low $k_1$ (<0.4): Integration of design, mask and lithography processes

Design For Manufacturing (DFM)

Application Specific Manufacturing

OPC & RETs: PSM, DPT, Scatterbars, DDL verification

Source-Mask Optimization

Application specific tuning

Litho aware design constraints

Design space

Manufacturing space

ASML
Matching using through pitch structures not adequate

Extended structure set required to capture all variations

Immersion matching performance between 1.2 NA and 1.35 NA system

A: 1900i-1700i Untuned baseline matching
B: 1900i-1700i Tuning based on pitch lines only
C: 1900i-1700i Tuning based on all patterns

Data generated in collaboration with IMEC
Integration of computational lithography tools
Source Mask Optimization & Litho double patterning

Traditional single clip Source Mask Optimization

Full-chip OPC & verification
SRAM + Logic optimized source
PW verification with Source 1

DOF = 82 nm EL = 10%

Final source

DOF = 98 nm, EL = 5%

Final PW has acceptable size

DOF = 98 nm, EL = 10%

Logic part of design

Split 1
Split 2

Split 1
Split 2

Cell design
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Improved (integrated) metrology & intra and inter-field control loops to drive CD and Overlay required

Tracking coat
Feedback
CD, OVL, Focus & Dose
Off-line metrology

Metrology system

Example intrafield CD control: “Dose mapper”

Inter-field: Dose per Field

Intra-field X-slit: Unicom

Intra-field Y-scan: Dosicom

Litho only can provide intra wafer/field control
High precision and productive metrology: angle-resolved scatterometry vs spectroscopic

Multi wavelength 2D vs 0D pupil detection for angle-resolved scatterometry for more process robust metrology

Angle-resolved scatterometry

Spectroscopic scatterometry

30x more photons for angle-based scatterometry for more productivity
Litho patterning process control for CD and Overlay of 32 nm, using angle-resolved scatterometry

Raw etched poly CDU

< 4.9 nm

< 7.0 nm

Line1

DoseMapper recipe

< 2.8 nm

< 3.8 nm

DoseMapper corrected etched poly CDU

< 0.8 nm

Mean CD

< 6.3 nm

Line2

DoseMapper recipe

< 6.3 nm

Overlay between litho 1 and 2

99.7% OVL X = 4.0 nm
99.7% OVL Y = 4.2 nm

Optimum GridMapper recipe

99.7% OVL X = 3.2 nm
99.7% OVL Y = 3.4 nm
Spacer double patterning: good line-width control

Line1
$3\sigma=2.1 \text{ nm}$

Line2
$3\sigma=2.0 \text{ nm}$

Space1
$3\sigma=2.1 \text{ nm}$

Space2
$3\sigma=4.1 \text{ nm}$

Line CD uniformity determined by spacer process

Space CD uniformity only partly correctable by litho: align main CD

Data generated in collaboration with IMEC
Correction of etch profile through dose improves space control

Uncorrected space spread

Dose corrected space spread

Data generated in collaboration with IMEC
Holistic litho optimization requires a combination of Computational and Wafer lithography.
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EUV producing the world first full field devices
SRAM cell and full working transistor

RHEM XP4502J
Alpha Demo Tool
EUV print

15GB 3D thick mask
panoramic simulation

Sample NMOS transistor
curve from EUV wafer

Reference
193 nm print of
SRAM bit cell

Full size AMD
Typhoon1

33 mm
22 mm

Albany Alliance
AMD IBM SONY TOSHIBA EUV Program
32 nm node SRAM contact patterning using EUV litho

55 nm dense and isolated contacts without OPC

Exposure Latitude

13.5 mJ 14.0 mJ 14.5 mJ 15.0 mJ 15.5 mJ

Litho
After Hard Mask etch
After Oxide etch

Data generated in collaboration with IMEC
Source roadmaps on critical path for TPT roadmap

Clean and spectrally pure photons

Power at IF (W)

- Supplier A
- Supplier B
- Supplier C

10 mJ/cm²
100 wph
10 mJ/cm²
60 wph
**EUVL Roadmap down to 11 nm**

support 22 nm and 16 nm node with a single projection system

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<tr>
<td>16 nm</td>
<td>same projection system, enhanced off-axis illumination</td>
<td>0.32 NA + off axis illumination</td>
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<tr>
<td>22 nm</td>
<td>0.32 NA, 3 nm OVL, &gt;100 wph</td>
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<tr>
<td>27 nm</td>
<td>0.25 NA, 4 nm OVL</td>
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Implementation volume production
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# Lithography system price evolution

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### Wafer Size
- 150mm
- 200mm
- 300mm

### Stepper
- i-line
- KrF
- ArF
- ArFi
- EUV

### Aperture
- 0.4
- 0.5
- 0.6
- 0.7
- 0.8
- 0.93
- 1.2
- 1.35

### Wavelength
- 0.25
- 1.35

Source: ASML
Litho cost per layer: estimates for 32 nm & 22 nm

Cost per layer set to increase

Reticle cost based on 5000 wafers / mask usage

ASML
ASML system throughput improvement drives CoO
Evolution in 300mm litho costs per layer

* Including chemicals, track, mask, deposition etc.

~10% average cost reduction / year

Year | Litho costs per single layer* [€]
--- | ---
2003 | 0.85 NA
2004 | 0.8 NA
2005 | 0.65 NA
2006 | 0.93 NA
2007 | 1.2 NA
2008 | 1.35 NA

ArFi | ArF | KrF | i-Line

* Including chemicals, track, mask, deposition etc.
NAND Memory: Cost Effective Shrink

Total litho cost per wafer (assuming greenfield fab) [€]

Relative cost NAND Memory Cell (4F²)

NAND Process Design Rule [nm]

35 mask layers
39 layers
41 layers
43 layers

Relative cost NAND Memory Cell (4F²) (70 nm = 1)
Double patterning will bridge the gap between single exposure 193 nm immersion and EUV.

- NAND Flash
- DRAM
- Logic

ASML product introduction:
- AT:1200
- XT:1400
- XT:1700i
- XT:1900i
- Next
- EUV
- Strong DPT

DFM supported low k1, light DPT

Year of Production Start*

*Process development 1.5 ~ 2 years in advance (updated 12/07)