“Moore’s Law….where next?”

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Bank of America Merrill Lynch
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Forward looking statements

This document contains statements relating to certain projections and business trends that are forward-looking, including statements with respect to our outlook, including expected customer demand in specified market segments (and underlying assumptions) including memory, logic and foundry, expected sales levels, trends, including trends towards 2020 and beyond and expected industry growth, and outlook, systems backlog, expected or indicative market opportunity, financial results and targets, including, for ASML and ASML and HMI combined, expected sales, other income, gross margin, R&D and SG&A expenses, capital expenditures, cash conversion cycle, EPS and effective annualized tax rate, annual revenue opportunity and EPS potential by end of decade and growth opportunity beyond 2020 for ASML and ASML and HMI combined, cost per function reduction and ASML system ASP, goals relating to gross cash balance and ASML’s capital structure, customer, partner and industry roadmaps, productivity of our tools and systems performance, including EUV system performance (such as endurance tests), expected industry trends and expected trends in the business environment, the addition of value through delivery of lithography products and the achievement of cost-effective shrink, expected continued lithography demand and increasing lithography spend, the main drivers of lithography systems, lithography intensity for all market segments, customer execution of shrink roadmaps, future memory application distribution, expected addressable markets, including the market for lithography systems and service options, expected manufacturing and process R&D, statements with respect to growing end markets that require fab capacity driving demand for ASML’s tools, statements with respect to the acquisition of HMI by ASML, including market opportunity, the expected timing of completion of the HMI acquisition and delisting of HMI, the expected benefits of the acquisition of HMI by ASML, including expected continuation of year on year growth, the provision of e-beam metrology capability and its effect on holistic lithography solutions, including the introduction of a new class of pattern fidelity control and the improvement of customers’ control strategy, statements with respect to EUV, including targets, such as availability, productivity, facilities and shipments, including the number of EUV systems expected to be shipped and timing of shipments, and roadmaps, shrink being key driver to industry growth, expected industry adoption of EUV and statements with respect to plans of customers to insert EUV into production and timing, the benefits of EUV, including expected cost reduction and cost-effective shrink, the expected continuation of Moore’s law, without slowing down, and that EUV will continue to enable Moore’s law and drive long term value, goals for holistic lithography, including pattern fidelity control, expectations relating to double patterning, immersion and dry systems, intention to return excess cash to shareholders, statements about our proposed dividend, dividend policy and intention to repurchase shares and statements with respect to the current share repurchase plan. You can generally identify these statements by the use of words like “may”, “will”, “could”, “should”, “project”, “believe”, “anticipate”, “expect”, “plan”, “estimate”, “forecast”, “potential”, “intend”, “continue” and variations of these words or comparable words. These statements are not historical facts, but rather are based on current expectations, estimates, assumptions and projections about the business and our future financial results and readers should not place undue reliance on them.

Forward-looking statements do not guarantee future performance and involve risks and uncertainties. These risks and uncertainties include, without limitation, economic conditions, product demand and semiconductor equipment industry capacity, worldwide demand and manufacturing capacity utilization for semiconductors (the principal product of our customer base), including the impact of general economic conditions on consumer confidence and demand for our customers’ products, competitive products and pricing, the impact of any manufacturing efficiencies and capacity constraints, performance of our systems, the continuing success of technology advances and the related pace of new product development and customer acceptance of new products including EUV, the number and timing of EUV systems expected to be shipped and recognized in revenue, delays in EUV systems production and development, our ability to enforce patents and protect intellectual property rights, the risk of intellectual property litigation, availability of raw materials and critical manufacturing equipment, trade environment, changes in exchange rates, changes in tax rates, available cash and liquidity, our ability to refinance our indebtedness, distributable reserves for dividend payments and share repurchases and timing of resumption of the share repurchase plan, and other risks indicated in the risk factors included in ASML’s Annual Report on Form 20-F and other filings with the US Securities and Exchange Commission. These forward-looking statements are made only as of the date of this document. We do not undertake to update or revise the forward-looking statements, whether as a result of new information, future events or otherwise.
Outline

• Moore’s Law – Where from → Where to?
• Drivers of demand for Moore’s Law
• ASML Enabling Moore’s Law for over 30 years
• EUV and the role it will play
• What’s next for EUV and ASML?
Moore’s Law


Moore’s Law visualization

So in real world terms what did Moore’s Law suggest?

Integrated circuits will lead to such wonders as home computers or at least terminals connected to a central computer, automatic controls for automobiles, and personal portable communications equipment.

40 years later

Selling Handy Home Computers between Notions and Cosmetics

G. Moore, "Cramming more components onto integrated circuits", Electronics, Vol. 38, Nb. 8 (1965)
Before 1965 a Moore’s Law like cadence was already being demonstrated…. computing speed/€ had been doubling every 2 years for about 65 years.
By the time ASML was founded Moore’s law was “in effect” for about 84 years.
Today Moore’s law has been “observed” for about 116 years…..so one might ask themself……..

Source: Ray Kurzweil
Why should it “SUDDENLY” stop now?

Source: Ray Kurzweil
"There's a law about Moore's law," jokes Peter Lee, a vice-president at Microsoft Research: "The number of people predicting the death of Moore's law doubles every two years".

Sturtevant's Law says that the end of optical lithography is 6 – 7 years away. Always has been, always will be.
The physical limits to computation have been under active scrutiny over the past decade or two, as theoretical investigations of the possible impact of quantum mechanical processes on computing have begun to make contact with realizable experimental configurations. **We demonstrate here that the observed acceleration of the Universe can produce a universal limit on the total amount of information that can be stored and processed in the future, putting an ultimate limit on future technology for any civilization, including a time-limit on Moore’s Law.** The limits we derive are stringent, and include the possibilities that the computing performed is either distributed or local.
After many unrecognizable calculations to most of us……….

Given the universal limit \( 2E/\pi \hbar \) on the number of operations per second that can be performed by all processors to determine the number of distributed operations:

\[
E_{\text{max}} = \frac{\Omega_m c^5}{128 G H \Omega^3_\Lambda} \left( 1 - \frac{3\Omega_m}{4\Omega_\Lambda} \right).
\]

If one assumes that each operation is of order of 1 bit, then the total

\[
E_{\text{max}}(R_*) = \int_0^{R_*} 4\pi R^2 dR \rho_M(R) \frac{E_a(R)}{E_e(R)}
\]

\[
= \frac{4\pi}{3} R_*^3 (\Omega_m \rho_c) [1 - (HR_*/c)]^3.
\]
Krauss and Starkman’s conclusion regarding our industry and Moore’s Law

“On a more concrete level, perhaps, our limit gives a physical constraint on the length of time over which Moore’s Law can continue to operate. In 1965 Gordon Moore speculated that the number of transistors on a chip, and with that the computing power of computers, would double every year [10]. Subsequently this estimate was revised to between 18 months and 2 years, and for the past 40 years this prediction has held true, with computer processing speeds actually exceeding the 18 month prediction.

Our estimate for the total information processing capability of any system in our Universe [8] implies an ultimate limit on the processing capability of any system in the future, independent of its physical manifestation and implies that...........

Moore’s Law cannot continue unabated for more than 600 years for any technological civilization.”

So…. I’ll let you decide!
Returning to the practical question……Why should it “SUDDENLY” stop now?
When long term multi-decade device roadmaps exist
Substantial performance gain next to the impact of geometric scaling

Every scaling innovation multiplies the value provided by our geometric scaling

Overall System Performance

Calculations per second per $1000

2012  2017  2022  2032  today

Source: John Kelly III, IBM, December 2015
Geometrical scaling critical in support of Moore’s law now enabled through 4 engines of innovations

Geometric scaling
2D shrink through patterning

Circuit scaling
System-on-chip and advanced packaging

Device scaling
New structures and materials

Architecture scaling
Solution optimization

Source: IMEC, customers
Logic device and shrink roadmap
New devices for 5 nm and beyond are demonstrated to work

<table>
<thead>
<tr>
<th>Year</th>
<th>Logic Device</th>
<th>Gate Length</th>
<th>Switching Threshold (mV/V)</th>
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<tbody>
<tr>
<td>2010</td>
<td>Planar</td>
<td>32 nm</td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td>FinFET</td>
<td>14 nm</td>
<td></td>
</tr>
<tr>
<td>2020</td>
<td>Horizontal Nanowire</td>
<td>5 nm</td>
<td></td>
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<tr>
<td>2025</td>
<td>Vertical Nanowire</td>
<td>~2.5 nm</td>
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<tr>
<td>&gt;2025</td>
<td>~1 nm</td>
<td></td>
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</tbody>
</table>

Improved performance

- FinFET (width 10nm)
- FinFET (width 5nm) lot 2
- GAA (lot 1, HIGH GP)

Nanowire device structure enables further reduction of gate lengths

Scaling of devices is enabled by materials innovation:
- High-K
- III-V

Source: IMEC (added to)
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Application trends in our industry drive continued demand for Moore’s Law

<table>
<thead>
<tr>
<th>Industry trends towards 2020 and beyond</th>
</tr>
</thead>
<tbody>
<tr>
<td>50B connected <strong>Internet of Things</strong> devices – needing low-cost devices and generating large data volumes requiring storage and processing</td>
</tr>
<tr>
<td>89 million <strong>connected cars</strong> on the road of which 6 million <strong>self-driving</strong> – generating and processing &gt;1 GB of data per second each</td>
</tr>
<tr>
<td>250 million <strong>personal health</strong> wearables and connected pharmaceuticals for health data collection</td>
</tr>
<tr>
<td>Explosion of <strong>(mostly unstructured) data</strong>, growing to &gt;40 Zetabytes from 5 Zetabytes today</td>
</tr>
</tbody>
</table>

...drive a reinforcing cycle of data creation, transmission, storage and processing...

- Very high volumes of **low-cost semicon devices**
- Massive **computing power and performance memory** in-cloud and in-vehicle
- Ultrafast & **high-band-width network infrastructure**
- Explosion of high-performance **storage capacity**

...driving demand for both **low-cost and high performance** semiconductor products in both memory and logic

...enabled by the **continuation of Moore’s law**...

...which underpinned by an **ecosystem** with combined profits of >290B$ 

Source: McKinsey, ASML
We operate in a highly profitable value chain with strong incentives to compete and drive innovation.

Top technology companies in our ecosystem (EBIT 2015, B$), source: S&P Capital IQ
5 tech predictions in the next 5 years, according to IBM

Tech giant reveals big predictions for technology by 2022, including superhero-like vision and detecting sickness early via mobile apps

**Artificial Intelligence (AI) will open a window into mental health**

*IBM predicts* that in five years, "What we say and write will be used as indicators of our mental health and physical well-being." For example, mental illness and disease such as Parkinson's could be detected sooner with a mobile phone app, thanks to AI calculations being done in the cloud. The sooner these conditions are spotted, the better placed we are to treat them.

**Superhero-like vision will be possible with Hyper-imaging, AI and new devices**

*According to IBM*, powerful, tiny cameras combined with the smarts of AI mean we’ll soon be able to literally see more than meets the eye by 2022.

In addition to visible light, we could see microwave, millimeter wave, and infrared images through devices small enough to fit in your pocket or clip onto a pair of glasses. Using this type of technology could allow you to instantly see whether food is safe to eat, and it could give self-driving vehicles the capacity to see through fog or rain more easily.
5 tech predictions in the next 5 years, according to IBM

(Cont)

We’ll understand Earth’s complexity in detail thanks to “macrosopes”

Being able to see a bird’s-eye view of anywhere on Earth is somewhat taken for granted now, thanks to satellite imagery. But Google Earth is just the beginning.

IBM predicts that “macroscope” systems, which are like microscopes but at the other end of the scale, are going to combine “all of Earth’s complex data together” so we can analyze it from new perspectives.

With this type of technology, we’ll be able to gather more data from satellites, smart sensors, and weather stations with an easier way to organize and sort through it all.

Labs-on-a-chip will revolutionize machinery

Computing technology has been shrinking, and it will continue to do so while becoming more powerful. According to IBM, this will largely benefit the medical industry. Imagine being at home, accurately diagnosing yourself at a low cost to catch and treat diseases earlier than ever.
5 tech predictions in the next 5 years, according to IBM (Cont.)

Smart sensors will quickly detect environmental pollution

IBM believes that the mix of smart hardware and AI analysis featured in its other predictions could also detect environmental pollution almost instantly. Similar to how a smart tracker could spot early signs of disease in the human body, smart sensors embedded in the ground or in drones could detect pollutants and emissions in real time without transferring samples back to a lab.
Huge Growth in Cloud Changes Semiconductor Supply Chain

By Paula Doe, SEMI
Solid State Technology

New layers and new types of memory

One likely change is new types and new placement speeds, different levels of non-volatile cache, and designs and accelerator subsystems that limit the need to move large amounts of data back and forth over limited pipelines. “Data is doubling every 2-2.5 years, but DRAM bandwidth is only doubling every 5 years. It’s not keeping up,” noted Steven Woo, Rambus VP, Systems and Solutions. “We’ll see the addition of more tiers of memory over the next few years.” He suggested the emerging challenge would be what data to place where, using what technology, and how to move memory in general closer to the processing. Racks may become the basic unit instead of servers, so each can be optimized with more memory or more processors as needed.

“Handling big data in the cloud means more opportunity for new memory technologies in an emerging tier between DRAM and solid state drives.” Source: Rambus
Large innovation ongoing in memory, driving continued litho demand

NAND displacing hard disks, 3D NAND displacing 2D NAND, albeit with significant integration challenges

Alternative technologies (e.g., CBRAM, PCRAM) likely high litho volume and performance

Source: Western Digital
Huge Growth in Cloud Changes Semiconductor Supply Chain

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Solid State Technology

Roadmap accelerates for networking chips

Look for accelerating change in the networking chip market. Now that merchant chip suppliers have taken over 75 percent of the networking chip market from the proprietary suppliers, intense competition in reducing size and power, and two-year technology cycles, reported keynote speaker Andreas Bechtolsheim, Arista Networks Chief Development Officer and Chairman.

"The cloud is accelerating transitions, as the big data centers demand low cost," he noted, explaining that new technologies no longer see gradual adoption through different applications. They have to start out cheaper to get any traction at all, but then ramp sharply to high volume in six months as high-volume data centers convert.

Bechtolsheim said the majority of the network link market will convert from 40G to 100G this year, and to 400G in 2019. For 800G two years later, chip design will have to start this year. Luckily there’s a clear path for scaling on the chip side, from the current generation’s 28nm technology down to 16nm and 7nm. But it could be a push for some of the ecosystem.

“It’s pushing the packaging vendors, as 1.0mm solder balls are about the limit,” said Bechtolsheim. Companies are also forming a group to speed the standards process by making the 800G standard simply 2X that for 400G, as the 400B standard took eight years.

The 40G chips at the server layer are moving to pulse amplitude modulation (PAM4) to send and receive four signals at once, which will require moving to digital signal processing. Moving from analog bipolar to digital CMOS technology also enables significant scaling of chip size and power, with significant reduction in die area (~50 percent) and power (~40 percent) with 16nm FinFET compared to 28nm, noted MACOM’s Chris Collins, director of Marketing. The company plans 7nm 800G devices next year.
In the end Jevons Paradox might help “explain” the present/future demand for Semiconductors.

**Jevons paradox** (/ˈdʒɛvənz/; sometimes the **Jevons effect**) occurs when technological progress increases the efficiency with which a resource is used (reducing the amount necessary for any one use), but the rate of consumption of that resource rises because of increasing demand.†

**Coal-burning factories in 19th-century Manchester, England.** Improved technology allowed coal to fuel the Industrial Revolution, greatly increasing the consumption of coal.

William Stanley Jevons (an English economist) in his 1865 book *The Coal Question*. 

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† Jevons paradox and Jevons effect are used interchangeably in this context.
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Lithography is at the heart of chip manufacturing and critical for shrinking transistors.

To produce a chip, the process is repeated ~50 times to build a 3-dimensional structure.
ASML enabling Moore’s Law for over 30 years (ASML’s whole history)

Semiconductor Industry Lithography Roadmap

Moore’s Law Observed over 40+ years
Lithography – Driver of Shrink

Lord Rayleigh

Rayleigh’s Equation

\[
\text{Resolution} = k_1 \times \frac{\lambda}{\text{NA}}
\]
Lithography – Driver of Shrink

Lithography shrink driver: reduce wavelength ($\lambda$), increase aperture (NA), lower $k_1$

Rayleigh’s Equation

$$\text{Resolution} = k_1 \times \frac{\lambda}{\text{NA}}$$

Lord Rayleigh

Increased Lens NA
Lithography – Driver of Shrink

Lithography shrink driver: reduce wavelength ($\lambda$), increase aperture (NA), lower $k_1$

Rayleigh’s Equation

$$\text{Resolution} = k_1 \times \frac{\lambda}{\text{NA}}$$

Lord Rayleigh

Reduce $k_1$ with Holistic Litho
Litho Shrink: 1400nm → 16nm, ~100x in 30 years

Enabled by shorter wavelengths, increasing NA and lower k1

Resolution = \( k_1 \times \frac{\lambda}{\text{NA}} \)

Source: ASML
Throughput: from 60 WPH (150mm) to 275 WPH (300mm) >30x increase in Silicon area exposed per hour

- **Wavelength**
  - EUV
  - Immersion
  - ArF
  - KrF
  - i-line
  - g-line

- **Wafer size**
  - 150 mm
  - 200 mm
  - 300 mm

- **Year of introduction**
  - 1985: PAS 2500 Stepper (1 M Euro)
  - 1990: PAS 5500 Stepper
  - 2000: PAS 5500 Scanner
  - 2005: TWINSCAN XTi
  - 2010: TWINSCAN NXT immersion
  - 2015: TWINSCAN NXE EUV (100 + M Euro)

Source: ASML
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EUV development has progressed over 30 years from NGL to HVM insertion.

- **1st lithography (LLNL, Bell Labs, Japan)**
- ASML starts EUVL research program
- ASML ships 2 alpha demo tools: IMEC (Belgium) and CNSE (USA)
- ASML ships 1st pre-production NA 0.25 tool NXE:3100
- ASML ships 1st NA 0.33 tool NXE:3300
- ASML ships 1st HVM NA 0.33 tool NXE:3400

Timeline:

- '85
- '86
- '87
- '88
- '89
- '90
- '91
- '92
- '93
- '94
- '95
- '96
- '97
- '98
- '99
- '00
- '01
- '02
- '03
- '04
- '05
- '06
- '07
- '08
- '09
- '10
- '11
- '12
- '13
- '14
- '15
- '16
- '17
- '18

USA: 5 μm

Japan: 160 nm, 80 nm

USA: 70 nm L&S, 28 nm Lines and spaces

NL: 19 nm Lines and spaces, 13 nm L/S

NL: 7 nm and 5 nm node structures
The future of lithography is EUV and it is here now.
Overcoming considerable challenges in the development of EUV

“We are continually faced by great opportunities brilliantly disguised as insoluble problems” – Lee Iococca

“The Wright Brothers flew right through the smokescreen of impossibility”
- Charles Kettering

Creating 30-cm diameter mirrors for use in our EUV lithography systems to a flatness specification of less than 2 nm across the total surface. If the mirror had the same diameter as the Earth, their tallest mountain would be just 9 cm high!

**Hitting** 20 micron droplets of tin, twice each, with a high power CO2 laser, at the rate of **50,000 droplets per second**, to create EUV light!

**Controlling** light beams so accurately it is equivalent to shining a torch from the Earth and hitting a 50 Eurocent coin placed on the moon!
So how does EUV help?...EUV delivers lower cost for complex patterning

LE3=Litho+Etch+Litho+Etch+Litho+Etch
Providing Customer Process Simplification

**Via hole patterning: immersion vs. EUV**

**EUV single patterning**
Combining patterns of all 4 immersion masks

**Lithography Situation**

ArF-i MPT hit the wall at 7nm

No. of masks $\uparrow$ → Cost $\uparrow$, Yield $\downarrow$, TAT $\uparrow$, Fab Capa $\downarrow$...

No. of masks

- L32
- L28
- L20
- L14
- L10
- L7
- L7(EUV)
As well as reducing cycle time and providing superior yield!!!!!

### Advantages of EUV Technology

#### Cycle Time Advantage

<table>
<thead>
<tr>
<th></th>
<th>Optical</th>
<th>EUV</th>
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</thead>
<tbody>
<tr>
<td>No. of critical masking steps</td>
<td>30</td>
<td>10</td>
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</table>

30 day reduced cycle time @ 1.5 days per masking level
- Cycle time reduction in development
- Cycle time reduction in manufacturing

#### Yield & Quality Advantage

- Less variation in electrical parameter
- Tighter process control

Source: GlobalFoundries-Gary Patton; ISS-Jan2017
When does it happen? - Industry Shrink Roadmap & EUV insertion

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<tr>
<td>Logic</td>
<td>20nm</td>
<td>16-14nm</td>
<td>10nm</td>
<td>7nm</td>
<td>5nm</td>
<td>3nm</td>
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<td>Performance Memory</td>
<td>28-30</td>
<td>20-22</td>
<td>1X</td>
<td>1Y</td>
<td>1Z</td>
<td>next</td>
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<tr>
<td>Storage Class Memory</td>
<td>Planar Floating Gate NAND</td>
<td>22</td>
<td>17-18</td>
<td>14-15</td>
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<tr>
<td>x24</td>
<td>x32</td>
<td>x48</td>
<td>x64</td>
<td>&gt;x96</td>
<td>&gt;x128</td>
<td>&gt;x192</td>
<td>&gt;x200</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Node name
Minimum half pitch
Minimum half pitch
/x number of layers

Source: 1) Customers - public statements, IC Knowledge LLC; 2) ASML extrapolations
What does it do? - EUV enables compelling cost down, returning to historic YoY cost/function levels (Moore’s Law)

Cost per function
Logic Flip Flop
(90nm = 100%)

- 90nm – 28nm: -24% YoY
- 28nm – 10nm: -18% YoY
- 10nm – 3nm: -22% YoY

Source: ASML, IC Knowledge, IMEC. Validated with external consultants
Cost and Complexity Down drives customer demand Up

"We plan to **extensively use EUV** in 5nm to improve density, simplify process complexity, and reduce cost...Recently EUV development gained quite a good momentum across the industry."
Mark Liu, co-CEO TSMC, July ‘16

"Samsung fully intends to **deploy EUV** for 7nm, triple patterning is not viable …"
"We expect production in 2018"
AnandTech & SemiconWest ‘16

"Significant strides have been made … taking the technology from a question of *if* to a question of *when*. **EUV is solidly on a path to HVM insertion** as soon as the technology becomes ready and cost effective"
Intel, SPIE ‘16

**EUV value**
€2 billion
18 systems
(Jan 2017)

**Technology**

- ArF Dry 3%
- KrF 9%
- I-line 1%
- EUV 50%
- ArF Immersion 37%

Q4’16 system Backlog
total value
€ 3,961 million

Source: ASML, public statements
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Our vision: Enabling affordable microelectronics

ASML's guiding principle is continuing Moore's Law

Our **vision** is to **enable affordable microelectronics** that improve the quality of life.

To achieve this, our **mission** is to **invent, develop, manufacture and service advanced technology for high-tech lithography, metrology and software solutions** for the semiconductor industry.

ASML's **guiding principle** is **continuing Moore's Law** towards ever smaller, cheaper, more powerful and energy-efficient semiconductors.

This **results** in **increasingly powerful and capable electronics** that enable the world to progress within a multitude of fields, including healthcare, technology, communications, energy, mobility, and entertainment.

*Fig. 1: The virtuous circle of the semiconductor industry*
# What’s next? - EUV extension roadmap

<table>
<thead>
<tr>
<th></th>
<th>55 WPH</th>
<th>125 WPH</th>
<th>145 WPH</th>
<th>185 WPH</th>
<th>Overlay [nm]</th>
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<tr>
<td>2013</td>
<td>NXE:3300B</td>
<td></td>
<td></td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>2015</td>
<td>NXE:3350B</td>
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<td>2017</td>
<td>NXE:3400B</td>
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<td></td>
<td></td>
<td>3</td>
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<td>&lt;2</td>
</tr>
</tbody>
</table>

- **At customer upgradable**
- **New platform**
- **Products under study**

- EUV extension roadmap
- NXE:3300B
- NXE:3350B
- NXE:3400B
- NXE:next
- High NA
ASML/Zeiss – Long time partnership as Two companies, One business

Securing the future of EUV

Sharing risk and reward, creating value for stakeholders
High-NA optics design concepts available
ASML invests in Carl Zeiss SMT to help secure the future

Resolution = $k_1 \times \frac{\lambda}{NA}$

Design examples

A Win/Win Situation …
Delivering value to customers drives ASML System ASP while reducing customer cost per function

- **Lithography revenue** is increasing (driven by number of wafer starts and higher lithography intensity) **while reducing the cost per function**

- For customers: **Cost per function reduction** (Logic):
  - -21% CAGR 2005-2015

- For ASML: **System ASP**: 8% CAGR 2005-2015

* ASML new systems revenue divided by new units recognized in a year
ASML Targets: 10B€ sales in 2020 … Sensitivities on 2020 ambition … 11B€ target with HMI but not included in this modeling exercise

<table>
<thead>
<tr>
<th>Market demand</th>
<th>ASML Sales in 2020</th>
<th>EUV insertion</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Worldwide units</strong></td>
<td><strong>(in B€/ ASP in m€)</strong></td>
<td><strong>Worldwide units</strong></td>
</tr>
<tr>
<td>High demand</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EUV 50</td>
<td>Systems 9.9</td>
<td>EUV 45</td>
</tr>
<tr>
<td>ArFi 80</td>
<td>Service &amp; Options 3.2</td>
<td>ArFi 50</td>
</tr>
<tr>
<td>Dry 145</td>
<td>Total 13.1</td>
<td>Dry 115</td>
</tr>
<tr>
<td>Total 275</td>
<td></td>
<td>Total 210</td>
</tr>
<tr>
<td>Low demand</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EUV 20</td>
<td>Systems 4.9</td>
<td>EUV 25</td>
</tr>
<tr>
<td>ArFi 50</td>
<td>Service &amp; Options 2.8</td>
<td>ArFi 75</td>
</tr>
<tr>
<td>Dry 90</td>
<td>Total 7.7</td>
<td>Dry 115</td>
</tr>
<tr>
<td>Total 160</td>
<td></td>
<td>Total 215</td>
</tr>
</tbody>
</table>

Reference ASML Investor Day 2016 presentation for more detail

Source: ASML, excluding HMI
We have significant leverage in our Financial Model …ASML and ASML + HMI combined

<table>
<thead>
<tr>
<th>Metric</th>
<th>2020 (Model)</th>
<th>2020 ASML/HMI combined (Model)</th>
<th>Driver HMI impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Sales</td>
<td>~10B€</td>
<td>~11B€</td>
<td>Combination of ASML/HMI, including associated new products, expected to increase our revenues in 2020 at higher than average ASML gross margin</td>
</tr>
<tr>
<td>Gross margin %</td>
<td>~50%</td>
<td>&gt;50%</td>
<td></td>
</tr>
<tr>
<td>R&amp;D % sales</td>
<td>~13%</td>
<td>~13%</td>
<td></td>
</tr>
<tr>
<td>SG&amp;A % sales</td>
<td>~4%</td>
<td>~4%</td>
<td>HMI product development supported by our current model</td>
</tr>
<tr>
<td>Capex % sales</td>
<td>~4%</td>
<td>~4%</td>
<td>Integration of HMI business not expected to have a significant impact on our Opex, Capex and Working Capital model</td>
</tr>
<tr>
<td>Cash Conversion Cycle</td>
<td>&lt;200 days</td>
<td>&lt;200 days</td>
<td></td>
</tr>
<tr>
<td>Effective Tax Rate</td>
<td>~13%</td>
<td>~14%</td>
<td>Reflecting different tax jurisdiction HMI</td>
</tr>
<tr>
<td>EPS</td>
<td>&gt;8€</td>
<td>&gt;9€</td>
<td>Combination of ASML/HMI expected to have a positive impact on EPS</td>
</tr>
</tbody>
</table>
Conclusions

- Opportunities for semiconductor device shrink continue to exist; **Moore’s law** is likely to remain an adequate description of the pace of computing-based technology innovation for the foreseeable future.

- Application trends and economics in our ecosystem are **driving increasing demand for processing power, high-speed memory, and low-cost storage**, fueling the continuation of **Moore’s law**.

- Continuation of Moore’s law will be supported by improved **patterning solutions**, achieving fast **yield ramp-up**, hence realizing **attractive economics**.

- Improving the single exposure resolution of lithography systems through the introduction of higher Numerical Aperture EUV systems remains the most **cost effective** way to enable device shrink.

- As a result, ASML’s strategic priorities are: **EUV industrialization**, **DUV competitiveness (not discussed today)**, leadership in **Holistic lithography (touched on today)** and **EUV extension** with High NA all underpinned with clear product roadmaps.

- The above underpins ASML’s long term growth opportunity through 2020 and beyond.
Thank You