Challenges in lithographic patterning of electronics structures on flexible substrates

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Contents

• Introduction Holst centre
• Introduction ‘lithography on flexible substrates’ program
• Results
  ▪ Foil characterization
  ▪ Handling of flexible substrates
  ▪ Imaging characteristics
  ▪ Transistor-on-foil demonstrator
• Conclusions
Holst Centre: Concept

- International open R&D centre, founded by IMEC and TNO
- Creating generic technologies, time to market 3..10 years
- *Wireless Autonomous Transducer Solutions* and *Systems-in-Foil*
- Shared programs with industry and universities
- Critical mass; 70 fte in 2006, 220 fte in 2010
Open Innovation at High-Tech Campus Eindhoven

- HTC initiated by Philips, now housing >50 companies
- Growing from 5000 to 8000 researchers
- Sharing of lab facilities (www.miplaza.com)
- New Open Innovation Research Centres (such as Holst Centre)
Systems-in-Foil: Sensing and Acting Foils/Films
## Systems-in-Foil: Programs

### Strategic programs:
windows on application areas, guiding choices in the technology programs

<table>
<thead>
<tr>
<th>Technology programs: Development of key technologies</th>
<th>Printed Organic Lighting &amp; Signage</th>
<th>Smart Bandage</th>
<th>Smart Blister</th>
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</thead>
<tbody>
<tr>
<td>Large Area Printing</td>
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<td>Electrodes and Barriers</td>
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<td>Foils Integration</td>
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<td>Printed Structures on Foil</td>
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<td>Organic Circuitry</td>
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<td>Litho on Flex substrates</td>
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Technology programs: having wider application than in selected application areas only (e.g.: PV, batteries, smart windows)

TP6 Lithography on flexible substrates, status wk804, E.R. Meinders, Confidential
Why flexible?

- Enhanced functionality for the end user: bendable, rollable, wearable devices

*But also*

- Integration of foil devices in products & systems: conformal application; convenient feeding into assembly system
- Efficient large area production of foil devices (e.g. roll-to-roll; no manual assembly)
The open innovation model

Shared R&D is a solution for the growing R&D costs (because of increased complexity)

1. Shorter time to market
2. Sharing ideas
3. Sharing of facilities
4. Leverage of R&D budget
Lithography on flexible substrates

Status technology program ‘Lithography on flexible substrates’
Erwin R. Meinders, Eindhoven, February 2008
Lithography on flexible substrates - products

- First E-book readers and mobile devices with flexible displays are being developed or close to market introduction:
  - Polymer Vision (~Q2 2008)
  - Plastic logic (~Q1 2009)
  - Seiko Epson
  - Samsung LCD
  - Universal display corporation
  - Flexible Display Centre
Global market forecast 2005-2025

Printed Electronics will be a Multi Billion $ Market
Source: IDTechEx, Organic Electronics Forecasts, Players, Opportunities 2005-2025

- 50% of market/applications @ 2025 requires micron-sized features
- Huge market potential for lithography on flexible substrates
Performance plastic electronic products

- Target feature size for plastic electronics is orders of magnitude away from state-of-the-art Si roadmap target.
Lithography on flexible substrates - main challenge

- Challenge: cope with both flatness and in-plane tolerances of flexible substrates
- foil stability is required for good overlay and registration
TP6 ‘lithography on flexible substrates’

Program objectives:

- Develop lithography technology for manufacturing of electronic circuitry on flexible substrates with (sub)-micron sized features.
- Develop technology together with all program partners (ASML, Philips, Bekaert, Singulus Mastering, Polymer Vision, TNO, IMEC, Mesa+).

Batch-to-batch, foil-on-carrier lithography:

- Feature size 1-10 μm, overlay accuracy < 1 μm.
- Use of mature optical lithography technology (MA6, PAS5500, etc).
- Foil-on-carrier approach for substrate handling.

Large area lithography:

- Develop a large-area, low-cost lithography technology for patterning of 2.5μm features for electronic applications on flexible substrates.
- Decisions need to be made with respect to equipment, lithography process, substrate handling, etc.
From foil-on-carrier towards large area lithography

lithography on flexible substrates roadmap

Foil on carrier
large area

2006 2007 2008 2009 2010 2011 2012
year

1/CD
From foil-on-carrier towards large area lithography: implementation

lithography on flexible substrates roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>Process and Patterning Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008</td>
<td>Screening/feasibility study</td>
</tr>
<tr>
<td>2009</td>
<td>Installation of large-area</td>
</tr>
<tr>
<td>2010</td>
<td>Release of large-area patterning equipment</td>
</tr>
</tbody>
</table>

- 10 \(\mu\)m CD, 3 \(\mu\)m overlay
- 5 \(\mu\)m CD, 1.5 \(\mu\)m overlay
- 1 \(\mu\)m CD, 0.3 \(\mu\)m overlay
- 0.5 \(\mu\)m CD, 0.15 \(\mu\)m overlay
Strategy: develop competences (building blocks) that address short and long-term objectives

lithography on flexible substrates roadmap

WP1: Foil characterization
WP2: Foil handling
WP3: process development
WP4: imaging/patterning
WP5: integration
TP6 access to excellent installed infrastructure (MiPlaza, Holst lab, MESA+)
Results
- foil characterization
- handling of flexible substrates
- imaging characteristics
- demonstrator

Status technology program ‘Lithography on flexible substrates’
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Foil deformation tester

- Measurement of in-plane mechanical deformation of flexible substrates

- Tester properties:
  - 5X microscope with automated stage
  - Method is based on detection of markers, resolution ~1 um
  - Foil size ~100x100 mm, via stitching

- In-situ measurement of foil deformation induced by lithographic process steps:
  - temperature exposure
  - solvent uptake
  - handling
Foil deformation tester

- Method based on markers (polystyrene spheres, laser-drilled holes, ink-jetted dots)
- Method calibrated with reference samples and validation experiments

Deformations minus the average displacements.

__Holst_40.txt
__Holst_80.txt
Foil deformation tester

Validation of experimental method via Finite element calculations.

In-plane deformation field: calculations (red arrows) and measurements

Effect of clamping: calculation (left) and measurement (right)

Conclusion: simulations support observed clamping artifact
Properties of flexible substrates

Measurement of Young’s and G modulus

Observation: good agreement for PEN foils, deviations for PET foils
Properties of flexible substrates

Study of anisotropy PET foil

<table>
<thead>
<tr>
<th>PET foil, thickness: 100 um</th>
<th>Position: middle</th>
<th>Position: middle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strain ($\varepsilon_y$)</td>
<td>$0.80 \cdot 10^{-03}$</td>
<td>$0.70 \cdot 10^{-03}$</td>
</tr>
<tr>
<td>Poisson’s ratio</td>
<td>0.27</td>
<td>0.30</td>
</tr>
<tr>
<td>$E$-modulus</td>
<td>5.46 GPa</td>
<td>6.13 GPa</td>
</tr>
<tr>
<td>$G$-modulus</td>
<td>2.14 GPa</td>
<td>2.36 GPa</td>
</tr>
<tr>
<td>External force direction</td>
<td>M.D.</td>
<td>T.D.</td>
</tr>
<tr>
<td>Experiment nr.</td>
<td>FC_EF_026</td>
<td>FC_EF_032</td>
</tr>
</tbody>
</table>

Observation: clear difference in mechanical behavior machine (MD) and transverse direction (TD)
Properties of flexible substrates

Influence of moisture uptake

Observation: linear relation between expansion and absorption
Handling of flexible substrates

Foil-on carrier lamination process to handle foil during lithography

Properties of lamination method:
• Separation at room temperature
• Good flatness performance
Handling of flexible substrates

Foil-on-carrier quality evaluated with PAS5500 high-resolution flatness measurements

Flatness measurement plot

Conclusion: lamination method yields an overall flatness of 1-3 micron
Handling of flexible substrates

Optimization of foil-on-carrier substrates preparation

Observation: bending is controlled by reduced foil thickness
Imaging characteristics: process

Patterning of micron-sized features on flex substrates with ASML PAS5500 wafer stepper

5 µm features @ wafer stepper
Optimization exposure power @ feature sizes (PAS5500 stepper)

Conclusions: good process window for micron-sized features on PEN foil
Imaging characteristics: process

Optimization focus/exposure power @ feature sizes (PAS5500 stepper)

Conclusions: good process window for 2 micron-sized features on PEN foil
Imaging characteristics: features size

Sub-micron imaging (on PAS5500 wafer stepper)

0.6 µm  0.4 µm  0.375 µm

Conclusion: feasibility submicron imaging on foil-on-carrier is demonstrated, process conditions to be optimized
**Imaging characteristics: overlay accuracy**

Alignment of layers is key for thin-film transistor on foil manufacturing

Pre-alignment markers in photoresist (left image) and metal (right image)

overlay accuracy <0.5 µm

Conclusion: good overlay registration (<0.5 µm) with foil-on-carriers
Transistor on foil demonstrator

Transistor array demonstrator: micron and submicron-sized transistors on PEN foil (collaboration with Holst Organic Circuitry program and IMEC)

Different stages in process

Conclusion: good overlay accuracy (<0.5 μm) and transistor performance
Transistor on foil demonstrator

Transistor array demonstrator: micron and submicron-sized transistors on PEN foil (collaboration with Holst Organic Circuitry program and IMEC)

Conclusion: good transistor performance w.r.t. V-I characteristics and mobility
Conclusions

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Conclusions

• Foil characterization competence in place to evaluate foil deformation due to solvent uptake, heat exposure and handling
• Foil-on-carrier lamination method provides excellent flatness and processing capability
• Micron-sized imaging on PAS5500 has good process window w.r.t. exposure power/focus and overlay performance (within 0.5 \( \mu \text{m} \)) for developed foil-on-carrier concept
• Imaging technology used to make transistor-on-foil demonstrator with good overlay and mobility characteristics
Thanks for your attention. Questions?

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