Productivity world records for i-line lithography

Extending KrF to reduce chip production costs

Double patterning for 32 nm production
Leading and emerging technologies such as immersion and EUV garner the lion’s share of public conversation, but old technologies (an exceptionally relative term in this case) are actually responsible for the majority of layers on today’s devices. i-line- and KrF-based scanners remain an integral part of today’s, and tomorrow’s, lithography process.

The modular design of ASML’s TWINSCAN lithography platform facilitates continuing development of each product line. This modularity also enables new technology products, in the form of system enhancements, to be retroactively applied for improvements in performance.

As a result of these ongoing developments, productivity of TWINSCAN i-line systems continues to rise, providing ever-increasing return on i-line technology investment. In September 2007, ASML issued a press release that detailed a record set by one of our Taiwanese customers. Specifically that they had imaged 3,596 wafers in a single day on an TWINSCAN XT:400F. As I write this (mid October) that record has already been beaten, and that one too.

Of course this type of productivity is only truly valuable when it is sustainable. Earlier this year a Korean customer realized an incredible achievement by imaging more than one million 300-mm wafers on one machine in one year.

This particular TWINSCAN i-line system imaged an average of more than 2,800 wafers per day for 365 consecutive days. Fantastic reliability.

In addition to i-line, KrF lithography systems continue to play a significant, and expanding role in chip manufacturing and will continue to do so for many years to come. This is why ASML recently announced the TWINSCAN XT:1000H, a high-productivity KrF scanner designed to minimize total fab ownership costs.

With the industry’s highest numerical aperture for a KrF system, it will offer a resolution of 80 nm. Providing this resolution on a KrF system will enable manufacturers to process more mid-critical layers in KrF even as technology nodes shrink, delivering cost-per-layer savings of 30% or more over ArF production.

Finally, and to appease the lions, I’d like to share the latest information on ASML’s immersion program. We have now shipped more than 60 systems worldwide. As of Oct 16, more than 4 million wafers have been processed on those systems. It’s time to focus on immersion.

As always I welcome your questions, comments or input at ryan.young@asml.com
Brion introduces lithography awareness to IC design flow

SANTA CLARA, California, May 28, 2007 — Brion Technologies, an ASML company, announced the availability of Tachyon Lithography Aware Design (LAD), an extension of the company’s Tachyon suite for optical proximity correction (OPC) verification and OPC application. Tachyon LAD gives designers of advanced integrated circuits (ICs) the ability to accurately assess how circuit designs will print on silicon under real-world production conditions.

ASML lowers chip manufacturing costs with new TWINSCAN XT:1000

SAN FRANCISCO, California – SEMICON West 2007 – July 16, 2007 – ASML announced a new KrF lithography system that significantly reduces operating costs for its customers. The ASML TWINSCAN XT:1000 scanner extends cost efficient KrF technology to resolutions that previously required more expensive ArF technology. Customers can realize savings of 30 percent or more per layer as a result of lower operating costs for KrF technology, particularly from cheaper lasers and lower materials cost such as KrF resists.
For complete information regarding these press announcements, please refer to the press section of www.asml.com.

ASML ships first lithography system for volume production of semiconductors with the world’s smallest features

VELDHOVEN, the Netherlands, July 18, 2007 – ASML announced that it has shipped its first TWINSCAN XT:1900i, the world’s only lithography system capable of imaging features down to 36.5 nanometers (nm) on chips manufactured in volume. Production of the TWINSCAN XT:1900i is now ramping up fast, as multiple orders have been placed and systems will be shipped before the end of this year to many of the world’s leading device makers.

Brion collaborates with STARC on its Tachyon-based workflow

YOKOHAMA, Japan, May 24, 2007 — Brion Technologies, an ASML company, in collaboration with Japan’s Semiconductor Technology Academic Research Center (STARC) will work to develop and test a complete design-for-manufacturing (DFM) workflow, enabled by Tachyon, Brion’s highly accurate and ultrafast optical proximity correction (OPC), resolution enhancement technology (RET) and OPC verification system.

ASML i-line scanners achieve new level of productivity Taiwanese customer processes record 3,596 wafers in single day

TAIPEI, Taiwan – SEMICON Taiwan 2007 – Sept 12, 2007 – ASML announced that a Taiwanese customer using its TWINSCAN i-line scanners has achieved an unprecedented level of 300 mm productivity by processing 150 wafers per hour for 24 hours, reaching a record output of 3,596 wafers in a single day.
Productivity world records for i-line lithography

By Marc Verdiessen

Abstract | Two ASML customers have recently set two very different productivity world records using our TWINSCAN i-line scanners. A Taiwanese customer produced 3,596 wafers in a single day on an TWINSCAN XT:400F, while a Korean customer recently announced it had processed more than 1 million wafers in a year on an TWINSCAN XT:400E.
TWINSCAN significantly boosts throughput by exposing one wafer while carrying out the metrology for the next. In addition, the TWINSCAN architecture is highly modular, allowing customers to feed developments from our leading-edge systems into their i-line tools.

This feature migration means TWINSCAN i-line systems offer best-in-class imaging as well as productivity, a vital consideration as technology nodes evolve. For example, even though the size of features printed in i-line isn’t changing, the smaller critical dimensions of advanced nodes makes i-line overlay performance much more important. The TWINSCAN XT:400 offers single-machine overlay (SMO) of 25 nm, while the TWINSCAN XT:450 pushes i-line SMO to 12 nm – and these values can be achieved at maximum throughput.

ASML is committed to pushing i-line as far as it can go. It’s this commitment that underpins the remarkable production records our customers are setting. It’s this commitment that is driving the growing popularity of our i-line systems in all markets. Several customers have chosen to add ASML i-line to fabs that already have ASML KrF and ArF systems. By using the same platform for all three wavelengths, they benefit from uniform automation and operator interfaces, optimal layer matching and, ultimately, higher yields.

Some people may think of it as “the old man” of lithography, but i-line technology is still hugely important to the industry. That’s why ASML continues to push forward both the performance and productivity of our i-line systems, to provide the maximum value of ownership throughout the fab.

3,596 wafers in a day
Our i-line tools’ excellent productivity was recently underlined when a Taiwanese customer set a new world record of 3,596 300-mm wafers in a single day using a TWINSCAN XT:400F. This averages out at 150 wafers per hour non-stop for 24 hours straight, 15 wafers per hour above the machine’s ATP throughput specification. Coincidently, it almost perfectly matches the ATP throughput specification for the next-generation TWINSCAN XT:400G, due to start shipping in November 2007.

The customer has only been using ASML i-line scanners for a year. Yet by optimizing its process, it was able to set a new world record on a base-model system, i.e., one with no additional throughput upgrades. 3,596 wafers in a day is a remarkable achievement. However, given the rate of growth for TWINSCAN productivity, this record will probably have been beaten by the time this magazine is printed.

One million wafers in a year
Earlier this year, Korean memory manufacturer Hynix announced it had produced over 1 million 300-mm wafers in a one-year period on an TWINSCAN XT:400E. This achievement was the result of several factors: the inherent capabilities of the TWINSCAN XT:400E, Hynix’s expertise in process optimization and the commitment of the ASML Korea customer support organization. It also demonstrates not just the high throughput of TWINSCAN i-line systems, but also their excellent reliability as it equates to producing 2,850 wafers per day – every single day for 365 consecutive days. And that can’t be done if the scanner is regularly unavailable.

150 wafers per hour non-stop for 24 hours

ASML is continually working to improve system availability for all lithography technologies. As well as reviewing the design and manufacture of our systems, we’ve introduced features such as WaitWatcher and Reticle Streaming that minimize dead time during lot processing through smart scheduling of routine tasks. In addition, our Smart Service program offers efficient, proactive support to increase productive time. With the 100th TWINSCAN i-line scanner shipping (to Hynix) in October, our global average i-line system availability is around 98%.

The secret to success
It’s no coincidence that these production records were set on ASML systems. As the only true dual-stage lithography platform, TWINSCAN significantly boosts throughput by exposing one wafer while carrying out the metrology for the next. In addition, the TWINSCAN architecture is highly modular, allowing customers to feed developments from our leading-edge systems into their i-line tools.

This feature migration means TWINSCAN i-line systems offer best-in-class imaging as well as productivity, a vital consideration as technology nodes evolve. For example, even though the size of features printed in i-line isn’t changing, the smaller critical dimensions of advanced nodes makes i-line overlay performance much more important. The TWINSCAN XT:400 offers single-machine overlay (SMO) of 25 nm, while the TWINSCAN XT:450 pushes i-line SMO to 12 nm – and these values can be achieved at maximum throughput.

ASML is committed to pushing i-line as far as it can go. It’s this commitment that underpins the remarkable production records our customers are setting. It’s this commitment that is driving the growing popularity of our i-line systems in all markets. Several customers have chosen to add ASML i-line to fabs that already have ASML KrF and ArF systems. By using the same platform for all three wavelengths, they benefit from uniform automation and operator interfaces, optimal layer matching and, ultimately, higher yields.

2,850 wafers per day – every single day of the year
Extending KrF to reduce chip production costs

by Frank Bomebroek

Abstract | The recently announced TWINSCAN XT:1000H is a high-productivity KrF scanner designed to minimize total fab ownership costs. With the industry’s highest numerical aperture for a KrF system, it will offer a resolution of 80 nm. Providing this resolution on a KrF system will enable manufacturers to process more mid-critical layers in KrF even as technology nodes shrink, delivering cost-per-layer savings of 30% or more over ArF production.
While systems like the TWINSCAN XT:1900Gi push the cutting edge of lithography forward, ASML is also applying our expertise to more mature technologies to reduce the total cost of ownership for our customers. The recently announced TWINSCAN XT:1000H is the latest example. Due for release in mid-2008, this high-productivity KrF scanner will offer resolutions of 80 nm and below – performance that was previously only available with ArF systems.

It will also include the TOP-3 package as standard, giving a single machine overlay of 6 nm and matched machine overlay of 10 nm – identical to TWINSCAN ArF systems. Moreover, as the first system on the new H platform, the TWINSCAN XT:1000H will offer throughputs up to 165 wafers per hour with further productivity upgrades already planned.

**Cutting mid-critical layer costs**

The TWINSCAN XT:1000H is primarily targeted at implant, metal and via layers. At the higher k₁ values used in these layers, the TWINSCAN XT:1000H is capable of resolutions from 95 to 110 nm as well as nodes further along the technology roadmap. Consequently, manufacturers will be able to keep more mid-critical layers in KrF as technology nodes advance, simplifying layer assignment between tools.

Moreover, KrF technology offers significant cost savings over ArF. KrF systems use less expensive optics and lasers, reducing the initial investment in tools. In addition, KrF resists are cheaper and lasers require less maintenance, so operating costs are also lower. As a result, the TWINSCAN XT:1000H helps manufacturers achieve cost-per-layer savings of 30% or more compared to ArF production.

**Taking KrF to the limit**

The TWINSCAN XT:1000H can offer such fine resolution thanks to its catadioptric lens design (one that includes mirrors as well as lenses). This is the first time such a design has been used in a KrF system, but the concept has already been thoroughly proven on over fifty hyper-NA ArF systems. The catadioptric design enables much higher NA values from compact assemblies and gives the TWINSCAN XT:1000H an NA of 0.93 – the highest for any KrF system in the industry.

In addition to the innovative lens design, the TWINSCAN XT:1000H is based on other proven technologies such as the AERIAL E illuminator used in the TWINSCAN XT:1400 and TWINSCAN XT:1450 ArF systems.

**Ideal for mid-critical layers in the 32 nm logic and 48 nm memory nodes**

from compact assemblies and gives the TWINSCAN XT:1000H an NA of 0.93 – the highest for any KrF system in the industry.

Moreover, KrF technology offers significant cost savings over ArF. KrF systems use less expensive optics and lasers, reducing the initial investment in tools. In addition, KrF resists are cheaper and lasers require less maintenance, so operating costs are also lower. As a result, the TWINSCAN XT:1000H helps manufacturers achieve cost-per-layer savings of 30% or more compared to ArF production.

**Specifications**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>NA</td>
<td>0.93</td>
</tr>
<tr>
<td>Resolution</td>
<td>80 nm</td>
</tr>
<tr>
<td>Laser power</td>
<td>40 W</td>
</tr>
<tr>
<td>Single Machine Overlay (SMO)</td>
<td>6 nm</td>
</tr>
<tr>
<td>Matched Machine Overlay (MMO)</td>
<td>10 nm</td>
</tr>
<tr>
<td>Throughput (50 mJ/cm²; 300 mm wafers, 125 fields, 16 x 32 mm)</td>
<td>165 wph</td>
</tr>
</tbody>
</table>
Double patterning for 32 nm production

by Frank van de Mast

Abstract | Double patterning is a bridge between today’s water-based ArF immersion and EUV technologies. By splitting complex patterns into multiple simpler ones, double patterning can greatly reduce $k_1$, to enable much finer resolution. Moreover, it can be carried out using existing resists and expose technology, making it the most likely solution for ramping-up 32 nm production by 2009.

Manufacturers are continuously shrinking IC design rules to improve performance or reduce die size (and hence cost). With simpler and highly periodic patterns, memory – and particularly NAND Flash – leads the way in feature shrinks. Assuming the current two-year cycle time for technology nodes continues, NAND Flash manufacturers will be looking to start 32 nm half-pitch production in 2009.

Current water-based immersion ArF technology enables production down to 40 nm half-pitch. Additional technology developments are needed to reach 32 nm. A number of directions have been suggested, including higher-refractive-index immersion and shifting to extreme ultraviolet (EUV) wavelengths. However, double patterning is increasingly seen as the most promising option for delivering 32 nm production within the 2009 timescale.

Seeing double

Double patterning involves splitting a dense chip pattern into two (or more) simpler mask patterns and printing each one as a separate layer. While the $k_1$ for each mask pattern is above 0.25 (the theoretical minimum value), the effective $k_1$ for the combined chip pattern can be much lower – leading to smaller features from existing lithography tools.

In the most straightforward implementation of double patterning (known as dual line), the first mask is exposed and etched into a hardmask film. The wafer is then coated with resist, and the second mask is aligned to the etched pattern then exposed and etched in the usual way. An alternative approach uses spacer technology to form self-aligned structures at sub-resolution feature size.

32 nm half-pitch production in 2009

The chief attraction of double patterning is the potential to reach 32 nm production by re-using existing water-based ArF technology and fab infrastructures.

There are, of course, still a number of technical and economic challenges, such as splitting chip patterns between
CD Uniformity for 32 nm lines using a dual line double patterning process

**32 nm lines: full wafer CDU 3σ = 4.5 nm**

![First population](image1)
![raw data: no filtering, no corrections](image2)
![Second population](image3)

<table>
<thead>
<tr>
<th>Litho exposure Equipment parameter as percentage of CD</th>
<th>Single exposure</th>
<th>Litho double patterning</th>
<th>Spacer double patterning</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔCD</td>
<td>7%</td>
<td>3.5%</td>
<td>3%</td>
</tr>
<tr>
<td>Overlay</td>
<td>20%</td>
<td>7%</td>
<td>20%</td>
</tr>
<tr>
<td>#mask steps</td>
<td>1</td>
<td>2</td>
<td>2-3</td>
</tr>
<tr>
<td># process steps relative to single exposure</td>
<td>1</td>
<td>2</td>
<td>3-4</td>
</tr>
</tbody>
</table>

40 nm dense CH  38 nm dense CH

EUV contacts using installed α tool with Xe source

Simple CD and overlay budget continued

multiple masks, increased cycle times through the fab and the cost of more critical-layer processing steps and masks. In addition, dual line double patterning requires extremely precise overlay while spacer double patterning demands finer CD control.

However, these challenges are by no means insurmountable. Our TWINSCAN XT:1900Gi has already demonstrated CD uniformity of 2 nm for 45 nm isolated lines and overlay below 3 nm in dedicated-chuck mode. Further overlay improvement is on the ASML roadmap for implementation in future systems.

In addition, ASML also supports research to address the other double patterning challenges. For example, researchers at IMEC are investigating techniques for automatically splitting chip patterns, creating “split-friendly” designs and reducing process costs.

**Beyond 32 nm**

Unlike higher-refractive-index immersion or EUV, double patterning doesn’t require the development of new resist or optical materials. It can also be carried out using existing lithography tools and fab infrastructure. Therefore, it should be production ready much earlier than the alternatives. Given realistic budgets for dose, focus, and overlay errors, double patterning using water-based immersion ArF systems has a practical limit of 22 nm half pitch for NAND Flash and 28 nm half pitch for complex ICs.

Beyond this, EUV is the likely option for volume manufacturing as it offers the greatest potential for further device scaling to even smaller features combined with the greatest possible cost of ownership. By bridging the gap between today’s ArF immersion scanners and mature EUV volume manufacturing tools of the future, double patterning is set to play a vital role in keeping the IC industry’s technology roadmap on schedule.
ASML rates high in VLSI’s Customer Satisfaction Survey

by Ryan Young

Abstract | ASML is committed to our customers. That commitment is reflected in the 2007 VLSI Customer Satisfaction Survey on Chip Making Equipment. For the fifth consecutive year, ASML has been awarded a place in the top three on VLSI’s “10 Best” list, the highest rating of any lithography exposure tool supplier.
How the VLSI Survey works

VLSI Research’s Customer Satisfaction Survey on Chip Making Equipment is the only public feedback forum available to the chip manufacturing industry. Manufacturers are able to rate their suppliers in thirteen categories: seven relating to equipment performance with six customer service categories. Every company receives a score between 1 and 10 for each category. For the 2007 survey, over 48,000 questionnaires were sent out worldwide in six different languages, meaning that about one in every sixteen employees in chip manufacturing was able to provide individualized feedback.

ASML’s Customer Commitment

ASML received high ratings in the two company categories that we are eligible for: Large Suppliers of Wafer Processing Equipment and Large Suppliers of Chip Making Equipment. This year our score of 7.71 placed ASML second overall exceeding last year’s score of 7.68. We strive not only to provide customers with leading technology, but also to ensure that they receive excellent customer service and support. The results of this survey provide us with valuable information about our progress in achieving these goals.

Ten Years in the 10 Best

ASML has been named one of the “10 Best” every year since 1998, and has placed in the top three in 8 of those 10 years. This year, we earned our highest Technical Leadership rating yet, the only Large Supplier of Chip Making Equipment to achieve a personal best score in a customer service category.

ASML’s rating over the last several years has shown steady growth in customer satisfaction, but this growth does not mean that we should not continue to work towards further improving customer support. Don Crabtree, SVP Sales states “There is no recognition or achievement more important to ASML than being recognized as a leader in customer satisfaction. Improving customer satisfaction is one of ASML’s corporate initiatives, and this survey result shows that while we continue to be rated highly, there is still room for further growth.”
ASML’s G-Force:

Great reliability, performance and value

by Carlo Battistella

Abstract | ASML has a history of continuous improvement to deliver the best possible value of ownership. With the latest G specification of our tried-and-trusted TWINSCAN dual-stage platform, we’re extending the trend towards higher commonality of parts and system availability. As a result, these new systems offer our best ever reliability, performance and value.

Our TWINSCAN systems may be industry leaders in productivity and performance, but that doesn’t mean that we’re just sitting back and relaxing. Instead, we’re continually looking at ways to evolve the platform to deliver even more. The latest G specification offers higher throughput, better overlay and a big step forward in reliability for the maximum value of ownership.

TWINSCAN is a highly mature lithography platform. By building on the strengths of its previous generations we can deliver additional significant performance improvements. To boost productivity, the new G systems feature even faster wafer and reticle stages, REMA and wafer handlers. In the TWINSCAN XT:875G, for example, this increases throughput by over 10% to 150 wafers-per-hour (wph) for 300-mm wafers. Moreover, the optional TOP-3 upgrade enables single machine overlay of 6 nm while running at full speed.

The common good

As with our previous platform evolution we’ve focused much of our development on increasing the level of commonality between systems. Now, over 80% of system modules are common across the platform and only wavelength- and node-specific components vary.

This commonality allows greater standardization of components, which has two key benefits. Firstly, it reduces the number of spare parts you need to stock and hence your operational costs. And secondly, it improves reliability for all our systems as there are fewer separate components to be developed and debugged.

Reliability comes as standard

As well as improving the platform itself, we’ve reviewed the way we actually go about developing and building machines. For example, we’ve intensified the Failure Mode and Effects Analysis (FMEA) program that we started with our F specification series.

As a result of these efforts, G specification systems have best-in-class system availability and reliability. For system availability, the specification has risen to 97%. Meanwhile, the reliability specification, measured in terms of mean time before interrupts (MTBI), has increased to 350 hours.

Maximum value

Of course, ASML’s end goal is to improve the overall value of ownership for semiconductor manufacturers. And we believe the G specification systems offer the best value yet. Their increased performance enables the manufacture of smaller and more complex ICs with higher yield. Similarly, their industry-leading throughput and outstanding availability allows manufacturers to achieve their production targets using fewer lithography clusters.

MTBI has increased to 350 hours
G Throughput improvements

Electrical Cabinets:
New power supplies & amplifiers

Rema:
Higher scanspeed, acceleration & jerk

Reticle Stage:
Increased scan speed, acceleration & jerk, reduced settling time and light-weight reticle chuck

Wafer Handler:
Input buffer and faster chuck swap

Wafer Stage:
Increased scanspeed to 600mm/s, increased acceleration & jerk and reduced settling time

Wafer Stage (measure side):
Faster wafer height map and faster alignment

G Overlay improvements

PALM:
Higher bandwidth lens vibration isolation control

Interferometer:
High speed Pressure correction

Airmounts:
Higher bandwidth frame vibration isolation control

Wafer Stage:
Continuously clamped wafer table

Level Sensor:
Level sensor MATCH2 standard

Airshowers:
Improved laminar flow airshowers
Abstract | In the history of lithography, the headlines usually go to developments in resolution. However, without parallel improvements in overlay, finer resolutions wouldn’t be any use to the semiconductor industry. Describing the accuracy with which a system can print a pattern directly on top of the pattern from the previous layer, good overlay performance is essential for high yield and to ensure the finished IC performs according to specification.
ICs are built up layer by layer, and modern ICs can easily have 30 or more layers. Overlay is a measure of a system’s ability to print these layers accurately on top of each other. Otherwise, electrical contact between structures will be poor and the resulting chip will not perform to specification and may not work at all. Overlay is a measure of the accuracy of this alignment. In short, without good overlay, you can’t have good yield.

But what is good overlay? Clearly that depends on the size of the features being printed – the smaller the features the more accurately you have to line them up. Traditionally, the rule of thumb was overlay performance should be better than one-third the critical dimension. So printing 65 nm features would require an overlay of approximately 20 nm. While this still holds for non-critical layers, manufacturers are already using one-sixth and looking towards one-tenth for critical layers.

Supporting this trend, ASML continues to make great strides in overlay performance with each new tool generation – delivering excellent overlay at the industry’s highest throughput. And thanks to our modular approach to system design, our overlay enhancements are often available for retrofitting in previously installed machines through our IOSc and IOSt packages for PAS 5500 and TOP packages for TWINSCAN systems.

Overlay definitions
For day-to-day manufacturing, what really counts is on-product overlay. However, this depends on process and design variables that vary from manufacturer to manufacturer and product to product. So in their product specifications, lithography system providers usually quote system overlay – achieved when printing standardized features under standardized conditions.

Single-machine overlay (SMO) is the overlay for two layers printed on the same system, while matched-machine overlay (MMO) is between different systems from the same manufacturer. For our dual-stage TWINSCAN systems, ASML often quotes a dedicated-chuck overlay (DCO), which is the overlay achievable if you print layers for a given wafer using the same stage. This feature is enabled through chuck dedication software.

Overlay budget contributions
Wafer and reticle alignment
One of the most important contributions to a system’s overlay performance is the ability to position and orient the wafer and reticle precisely. This is known as (wafer / reticle) alignment and relies on the detection of alignment marks on the wafer or reticle. ASML has been a leader in alignment ever since we were founded.

In our very first commercial system (released in the early 1980s), we introduced through-the-lens (TTL) wafer alignment.

Our newer systems feature the ATHENA advanced alignment technology, which detects more diffraction orders and uses both red and green light. This enables greater alignment accuracy and improves overlay for even the most difficult process stacks. In addition, the Reticle Blue Align feature uses blue 193 nm light and an integrated transmission image sensor to ensure the mask is correctly aligned to the wafer stage without requiring a separate wavelength calibration step.

Wafer distortion
Once the wafer is aligned on the chuck, it needs to be clamped in the correct position. Wafer clamping can stress the wafer causing it to deform and affecting overlay performance. ASML uses a vacuum clamping process to minimize the stress and hence distortion. However, wafer distortion can also occur in many non-lithography process steps. Our recently released GridMapper option compensates for any wafer distortion to improve on-product overlay performance.

Excellent overlay at the industry’s highest throughput
The performance of a photolithography tool is characterized by three key capabilities. Imaging, or the ability to consistently resolve small features, governs the IC’s size (hence cost) and performance. Overlay describes how accurately a system can print consecutive layers on top of each other. This affects the performance of the IC and the yield of good dies per wafer. Finally productivity, measured by how many wafers a system can process in a fixed time, impacts on the cost of the IC and the manufacturer’s profitability.

The next edition of Images, we will be taking a closer look at productivity.

System calibration and control
Alignment ensures the reticle and wafer are correctly positioned on the appropriate stage. However it is also important to ensure the stages themselves are correctly positioned within the machine before exposure. To achieve this, the system must have excellent control of the motors that move the wafers around, which is usually governed through interferometers to measure the stage’s position.

Different lithography technologies have different wafer environments. In i-line and (dry) DUV lithography, the wafer is surrounded by air. In immersion, it is surrounded by water (or potentially another liquid) and EUV lithography requires a vacuum. So each technology presents unique challenges. However, building on our excellent overlay performance in dry systems, ASML has managed to maintain the overlay roadmap as the industry starts to adopt immersion. Our system control know-how will also prove beneficial in the future transition to EUV.

Enabling smaller features
Overlay improvements have always been essential to support finer system resolutions in the quest for smaller features. Now, however, overlay is playing an intrinsic role in driving feature size through techniques such as double patterning. Double patterning involves

Our overlay enhancements are often available for retrofitting in previously installed machines
splitting the circuit pattern into two simpler patterns that are printed in successive steps.

Currently the subject of much research and a promising candidate for 32 nm production (see article page 10), double patterning requires extremely accurate overlay – within a few nanometers. Our latest systems already have SMO specifications as low as 6 nm and DCO as low as 3 nm at resolutions from 40 to 85 nm, and future stage control and alignment sensor developments will enable further overlay gains. This will not only make double patterning a viable production technology, it will greatly improve performance and yield for all technology nodes.

In the next and final article in this series, we’ll be looking at productivity – or how to make process wafers in less time.

Example of on-product overlay: Wafer alignment marks in eighth metal layers are stacked on top of each other

Due to many non-lithography process steps wafer distortion can occur. GridMapper can correct for these errors

Example of double patterning overlay: Overlay within one layer becomes part of the critical dimension uniformity

Our latest systems have SMO specifications as low as 6 nm
www.asml.com

Corporate Headquarters
De Run 6501
5504 DR Veldhoven
The Netherlands
Phone +31 40 268 30 00

U.S. Main Office
8555 South River Parkway
Tempe, AZ 85284 USA
Phone +1 480 383 4422

Asia Main Office
Suite 1702-3 17th Floor
100 Queen’s Road Central
Hong Kong,
Hong Kong, SAR
Phone +852 2295 1168